

YTM32B1MD2x Data Sheet

Support: YTM32B1MD24H0MLLT, YTM32B1MD24H0MLHT, YTM32B1MD24H0MLFT

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1 Features Summary

- AEC-Q100 qualified
- ASIL-B compliant
- RoHS compliant
- 32-bit Cortex-M33 with FPU and DSP, up to 80 MHz
- Debug functionality
 - Joint Test Action Group (IEEE 1149.1 standard)
 - Serial Wire Debug (SWD)
- Up to 256KB * 2 Program Flash (PFlash0/1)
 - Support ECC feature
 - Support OTA
 - Wide operating voltage ranges (2.97 ~ 5.5V) with fully functional Flash memory program/erase/read operations
- Up to 64KB DFlash
- Up to 4KB Cache
- Up to 64KB SRAM
 - Support ECC feature
- 8KB on-chip ROM supports secure boot
- Provide multiple clock sources including:
 - 48MHz Fast Internal RC Oscillator (FIRC)
 - 2MHz Slow Internal RC Oscillator (SIRC)
 - 4~40MHz Fast Crystal Oscillator (FXOSC)
 - 32KHz Low Power Oscillator (LPOCLK)
 - 80MHz Phase-Locked Loop (PLL)
- Power Control Unit (PCU) with internal regulators capable of supporting multiple power modes including:
 - Active
 - Sleep
 - Deepsleep
 - Standby
- 8 DMA channels with up to 64 hardware trigger sources
- Analog modules providing precision mixed-signal capabilities, including:
 - One 12-bit, 1Msps SAR eADC, up to 32 external channels and 4 internal channels
 - On-chip Analog Comparator (ACMP) with 8-bit DAC, up to 8 channels
 - Temperature sensor
- Timers
 - One 4-channel Periodic Timer (pTMR)
 - One Low Power Timer (lpTMR)
 - Two 8-channel Enhanced Timer (eTMR)
 - One 16-channel Multiple Pulse Width Modulation (MPWM)
 - One Real Time Clock (RTC)
- Serial communication interfaces
 - Three FlexCAN modules with FD
 - Three UART modules
 - Three SPI modules, support I2S
 - Two I2C modules
- Security and Safety features are supported as follows:
 - Cyclic Redundancy Checker (CRC)
 - Hardware Cryptography Unit (HCU) which supports AES-128(ECB/CBC/CMAC), SHA-256, RSA-1024/2048/3072/4096 and ECC-192/256/384
 - True Random Number Generator (TRNG)
 - Clock Monitor Unit (CMU)
 - Clock Frequency Measure Unit (CFMU)
 - Watchdog (WDG)
 - External watchdog (EWDG)
 - ECC Management Unit (EMU)
- Human-machine interfaces
 - Up to 88 General-Purpose Input/Output (GPIO)
 - External interrupt
- I/O supporting 2.97 ~ 5.5V supply
- Temperature range:
 - Ambient operating temperature: -40 °C ~ 125 °C
 - Junction temperature: -40 °C ~ 150 °C
- Package options
 - 100-pin LQFP
 - 64-pin LQFP
 - 48-pin LQFP

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2 Overview

The YTM32B1Mx is a family of microcontrollers built on the latest ARM® Cortex®-M33, and it offers a broad range of memory, peripherals and package options.

The YTM32B1Mx family introduces new features and uses high performance, high reliability CMOS technology to provide substantial cost reduction and significant performance improvement.

YTM32B1MD2x series of devices are 32-bit general purpose automotive microcontrollers based on the ARM Cortex-M33 core. They offer superior performance, large memories and the most scalable peripherals in this class. This product series provide up to 80 MHz CPU performance, with up to 512KB PFlash, 64KB DFlash, 8KB ROM and 64KB SRAM.

3 Block Diagram

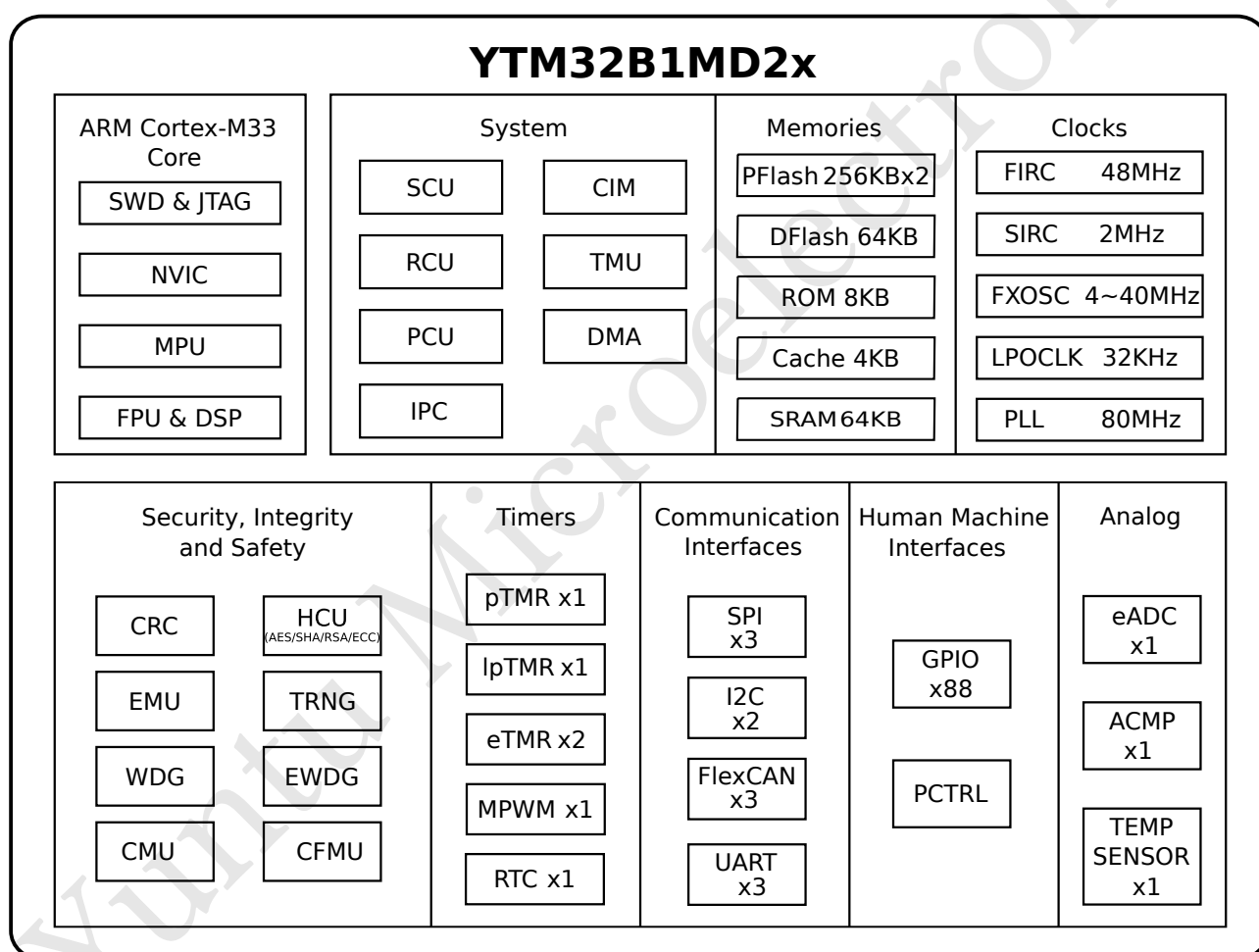


Figure 1: YTM32B1MD2x Block Diagram

4 Features

The following sections describe the high-level module features for YTM32B1MD2x device.

4.1 Core Modules

4.1.1 ARM Cortex-M33

- An in-order issue pipeline.
- Thumb-2 technology.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor.
- A Floating Point Unit (FPU) supporting single-precision arithmetic.
- Support for exception-continuable instructions, such as LDM, LDMDB, STM, STMDB, PUSH, and POP. If the processor supports FPU, the VLDM, VSTM, VPUSH, VPOP exception-continuable instructions are also included.
- Low-power features including architectural clock gating, sleep mode, and a power aware system with optional Wake-up Interrupt Controller (WIC).
- A memory system, which can include optional memory protection and security attribution.
- Support multiple regions MPU.

4.2 System Modules

4.2.1 System Clock Unit (SCU)

- Fast internal RC oscillator(FIRC)
 - Up to 48 MHz
 - Default system boot clock source
 - Support trim for temperature and process
- Slow internal RC oscillator(SIRC)
 - Up to 2 MHz
 - Can be selected as system clock source
 - Always on unless it is forced to be disabled in Deepsleep and Standby mode
 - Support trim for process
- Fast crystal oscillator(FXOSC)
 - Support 4~40 MHz crystal
 - Can be selected as system clock source
- Low power oscillator(LPOCLK)
 - 32 KHz always on clock source
- Phase-Locked Loop(PLL)
 - Up to 80 MHz
 - Contains voltage-controlled oscillator(VCO)
 - Support selectable reference clock
 - Contain frequency lock detector
 - Can be selected as system clock source
- SCU provides glitch free switcher to select system clock source
- SCU provides system clock dividers to generate core clock, fast bus clock and slow bus clock.

4.2.2 Power Control Unit (PCU)

- Combination of internal and external voltage regulator options, offering a variety of power modes
- Active POR providing brown-out detect
- Low voltage reset for all system relevant power domains (LVR)
- Low voltage detect (LVD) as an indication for software.

4.2.3 Reset Control Unit (RCU)

- Record the reset sources of most recent resets.

- Configurable filter for reset pin.
- Reset pin filter can work in Active, Sleep, Deepsleep , Standby mode.

4.2.4 IP Control (IPC)

- Peripheral Bus clock enable
- IPC clock source selection from multiple clock sources
- IPC clock divide values from 1 to 16
- Peripheral software reset

4.2.5 Direct Memory Access (DMA)

- All address range data transfer from source to destination
- Support separate source/destination data size configuration
- 32-byte 16-byte burst and Double word(64-bit) Word(32-bit), half word(16-bit), byte(8-bit) transfer size
- Support separate source/destination address offset configuration
- Address increase/decrease/keep selectable
- Up to 8 DMA channels
- Fix priority and round-robin arbitration
- Support channel to channel link
- Software/Hardware/Link trigger
- Up to 64 peripheral hardware triggers
- Internal data FIFO for data transfer
- Support update DMA transfer information from system memory after transfer complete
- Support data transfer loop and trigger loop

4.2.6 Trigger Multiplexer Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources

4.2.7 Chip Integration Module (CIM)

- System function configuration
- ACMP trigger synchronize selection
- Software trigger generate
- eTMR external clock and fault selection
- FPU interrupt enable
- Flash memory and system RAM size configuration
- Package configuration

4.2.8 CACHE

- 2-way set associative
- 4 word line size
- Lines can be invalidated individually
- Entire cache can be invalidated at once
- Cache supports write through
- Cache parity error control and report

4.3 Memories

4.3.1 Embedded Flash Module (EFM)

- Program Flash (PFlash) support 512KB address space
 - PFlash support ECC 1-bit error correction and 2-bit error detection (SEC-DED)
 - Support Read-While-Write and OTA (Over-The-Air) technology
- Data Flash (DFlash) support 64KB address space
- Protection scheme against accidental program or erase operations
- Command protection function for authorization protection
- Optional interruptions on command completion and status update

4.3.2 Read-Only Memory (ROM)

- 8KB on-chip memory map
- The ROM boot firmware is programmed by YTMicro to support the following three functions: Secure Boot, system clock and watchdog configuration:
 - Run once the chip releases the reset signal of the CM33 core
 - Support the parsing of the configurable BVT (Boot Vector Table) stored in the Flash memory
- Secure Boot
 - Work as the root of trust
 - Support CMAC authorization of the customized code (i.e. bootloader, OTA) with the specified secure boot group configuration set in the BVT. (Note: The CMAC authorization is achieved by HCU.)
 - * Support decryption of secure boot section configuration structure with the specified HCU AES key in secure boot group configuration
 - * Support up to 8 secure boot section configurations (each includes the section start address, length and HCU AES key used for CMAC as well as CMAC stores address pointer)
 - The used HCU hardware user keys for secure boot section configuration structure encryption and CMAC authorization should be pre-programmed to HCU_NVR memory by the Car OEM or Tier-1 using the flash programmer
 - Support strict serial secure boot mode (enabled via BVT)
 - * If CMAC authorization fails, the secure boot holds the CM33 core in static mode
 - Support normal serial secure boot mode (by default)
 - * If CMAC authorization fails, the CM33 core continues to execute the bootloader and the applications, but all HCU hardware user keys will be disabled or fail to load.
- System clock configuration
 - Support flexible system clock configuration for ROM boot via BCW in BVT. For example, using 80MHz PLL rather than the default 48MHz (FIRC) can reduce the boot time.
 - Support flexible core clock divider for ROM boot via BCW in BVT.
- Watchdog configuration
 - Support watchdog enable/disable function.
 - Support timeout configuration for CM33 main core.
 - Support watchdog clock source select.

4.4 Analog

4.4.1 Enhanced Analog-to-Digital Converter (eADC)

- Contain 1 eADC instances
 - eADC0 supports up to 32 external analog input channels, and 4 internal channels
- Support 12-bit, 10-bit, 8-bit and 6-bit single-ended configurable resolution
- Up to 1 Msps for 12-bit resolution conversion performance

- Support high-priority sequential DMA and low-priority sequential DMA requests
- Support multiple conversion modes
 - Single mode
 - Continuous mode
 - Discontinuous mode
- Support software/hardware trigger for eADC start conversion, High-priority sequences can be triggered by the corresponding hardware; low-priority sequences can be triggered either by software or by the corresponding hardware; high-priority sequences can preempt low-priority sequences being converted at any time
- Support power saving modes
 - Auto off mode: automatic control eADC power off
- Support watchdog for conversion result monitoring
- Support different high-priority sequence and low-priority sequence assignment schemes
- Support sampling average
- Support variable sample rate switching
- Each channel in the sequence corresponds to its own buffer, which can be read freely
- Support configuration of data overflow per channel
- Support interrupt generate
 - Ready for conversion
 - End of sampling
 - End of conversion
 - End of high-priority sequence conversion
 - End of low-priority sequence conversion
 - Overrun event
 - Watchdog event
 - High-priority and Low-priority trigger source loss error event
- Support work and wake up when the chip is under sleep and deepsleep modes

4.4.2 Analog Comparator (ACMP)

- Up to 8 channels
- Operational over the entire supply range
- ACMP DAC Buffer inputs may range from rail to rail
- Programmable hysteresis control
- Selectable inversion on comparator output
- Function mode:
 - Common mode
 - Sample mode
 - Window mode
 - Continuous mode
 - * One-shot mode
 - * Loop mode
- All channels can be used to execute automatic comparison
- Support digital filter, the filter can be bypassed

- Two software selectable performance levels
 - Shorter propagation delay at the expense of higher power
 - Low power with longer propagation delay
- Functional in all power mode
- Support independent 8-bit DAC output to the comparator
- Support DAC_OUT 5v to pad
- Support several interrupts
 - For common/sample/window mode
 - * Generate interrupt on rising-edge, falling-edge or both edges of the comparator output or generate interrupt when comparator output is high or low
 - For continuous mode
 - * Generate interrupt when the comparison results don't match with expectations
- Interrupt can be generated without any clock in common mode
- A comparison event can be selected to trigger DMA transfer

4.5 Timer

4.5.1 Periodic Timer (pTMR)

- Timers can generate interrupts, and each channel can generate interrupt request
- Four channels of 32-bit timers, each timer has independent timeout periods
- Ability to stop in debug mode
- Support chain mode to connect multiple timer to a longer timer
- Timer can select bus clock or function clock as timer clock source, default is bus clock
- Timers can generate trigger, and each channel can generate its trigger

4.5.2 Low Power Timer (lpTMR)

- 16-bit time counter or pulse counter with compare
- Optional interrupt can generate asynchronous wakeup from any Low-power mode
- Hardware trigger output
- Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
 - Rising-edge or falling-edge
- Generate DMA request when counter reach compare value

4.5.3 Enhanced Timer (eTMR)

- Configurable initial and final counter values
- Contain 8 channels
- Support two clock sources
 - Bus clock
 - External clock
- Support 7-bits clock prescaler
- Support four channel modes
 - Common timer
 - PWM mode

- * Independent mode for each channel
- * Complementary mode for each pair of channels
 - Odd channels and even channels support independent deadtime insertion
- * Support dithering
- * Channel output control (initialization, software control, mask control, double switch control, fault control)
 - Support 4 fault input sources
 - Support fault input from TMU or pad
 - Support fault input polarity control
 - Support fault input filter
 - Support fault input stretch
 - Support fault event generated by combinational logic
- * Relevant registers have buffer registers and support loading mechanism
- Output Compare mode
 - * The output can be configured to set, clear or toggle on match point
- Input Capture mode
 - * Support rising edges, falling edges or dual edges capture
 - * Support input filter with a prescaler
 - * Support capture test mode
 - * Support pulse width measure
- Support generating triggers
 - Output triggers with adjustable pulse width on match point
 - Output pulse with adjustable width by PWM
- Polarity control is available for each channel
- Support GTB (Global Time Base)
- Support several interrupts
 - Channel interrupt (capture interrupt and compare interrupt)
 - Counter overflow interrupt
 - Fault event interrupt
- Support DMA
- Support counter running under debug mode
- Support input from ACMP

4.5.4 Multiple Pulse Width Modulation (MPWM)

- Each MPWM supports 16 channels
- Each channel contains a 16-bit counter independently
 - Configurable comparison value
 - Configurable period value
- Support clock prescaler(1, 2, 4, 8, 16, 32, 64, 128) independently
- Counting modes
 - Continuous mode
 - One shot mode
- Support counter starts counting by hardware trigger in one shot mode
- Support four channel modes
 - Common timer

- PWM mode
 - * Independent mode for each channel
 - * Support edge-aligned PWM
 - * Relevant registers have double buffer registers and support loading mechanism
 - * Write operations to double buffer registers take effect immediately
- Output Compare mode
 - * The output can be configured to set, clear or toggle on match point
- Input Capture mode
 - * Support rising edge capture
 - * Support falling edge capture
 - * Support any edge capture
 - * Support combination capture
- Pulse count mode
- Center-Aligned mode
- Support generating triggers on match point
- Polarity control is available for each channel
- Support several interrupts
 - Channel event interrupt
 - Timer overflow event interrupt
- Support DMA
- Support hall sensor input
- Support input from ACMP
- Support counter running under debug mode

4.5.5 Real Time Clock (RTC)

- Register write protection for RTC enable register
- 32-bit seconds counter with overflow flag, second flag and their optional interrupt
- 32-bit alarm register, support report alarm flag and optional interrupt
- Configurable 1, 2, 4, 8, 16, 32, 64 or 128 Hz square wave output with optional interrupt
- Software reset for all register
- Support enter debug mode
- Support select clock source for counter, and support select output clock source

4.6 Security, Integrity and Safety

4.6.1 Cyclic Redundancy Check (CRC)

- The following CRC polynomials are implemented:
 - CRC4 (CRC-ITU):
$$X^4 + X + 1$$
 - CRC8 (CRC-ITU):
$$X^8 + X^2 + X + 1$$
 - CRC16 (CRC-CCITT):
$$X^{16} + X^{12} + X^5 + 1$$
 - CRC32 (CRC-ethernet):
$$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$
- Programmable initial seed
- Optional bit-swap in one byte is available for input data
- Optional bit-swap in one word is available for output data
- Optional bit-inversion is available for output data

- 8/16/32-bit access for CRC input data

4.6.2 Hardware Cryptography Unit (HCU)

- Support 128-bit key length
- Support both encryption and decryption
- Support secure hardware key and flexible software key
- Support several algorithm engines
 - AES (ECB, CBC , CMAC)
 - SHA (SHA-256)
- Support separate public key algorithm accelerate engine (PKE)
 - RSA (1024/2048/3072/4096)
 - ECC (192/256/384)
- All data input/output are in little-endian format
- Support bit, byte and half-word data swapping
- Support DMA transport
- Support several interrupts
- Clock gating strategy is applied for engine core

4.6.3 True Random Number Generator (TRNG)

Features of the TRNG module include:

- Generate a 128-bit entropy
- Monobit test to limit the number of value 0 and 1
- Long run test to avoid continuous constant value
- 1 ring OSC with clock checker
- 3 interrupt source
 - Entropy valid interrupt
 - Frequency error interrupt
 - Hardware error interrupt

4.6.4 ECC Management Unit (EMU)

- Independent channel of ECC injection and report for each memory array
- Two-stage enable mechanism for ECC injection
- Correctable or uncorrectable error can be injected
- Each channel's ECC error interrupt can be enabled with separated register bit
- The last ECC error data can be recorded into register

4.6.5 Clock Monitor Unit (CMU)

- CMU support maximum 8 channels that can continuously monitoring clock nodes concurrently
- Each CMU channel can continuously monitoring clock out-of-range and clock miss
- CMU initiates an out-of-range event if monitored clock frequency higher than high frequency limitation
- CMU initiates an out-of-range event if monitored clock frequency lower than low frequency limitation
- Out-of-range event reports to system with asynchronous interrupt or asynchronous reset
- CMU initiates an clock-miss event if monitored clock loss

- CMU initiates an clock-miss event if reference clock loss
- Clock-miss event reports to system with asynchronous reset
- Each CMU channel optionally support detecting over-time delay between monitored clock enable and monitored clock valid
- CMU initiate a clock-valid-miss event if has not get monitored clock valid in configured time limitation
- Clock-valid-miss event reports to system with asynchronous reset

4.6.6 Clock Frequency Measure Unit (CFMU)

The Clock Frequency Measure Unit includes two 16-bit counters, one connected to the bus clock and the other selectable via a control register to measure on-chip clock sources.

- An 8-bit divider is provided to ensure the to-be-measured clock can be measured relative to the bus clock.
- A target count register for both the reference(bus) clock and to-be-measured clock are provided to stop the counters.
- The to-be-measured clock can be configured to output to pad

4.6.7 Watchdog (WDG)

- 16-bit countdown timer
- Functional clock can be selected from multiple clock sources
- Support regular or window servicing mode
- Support reset request or interrupt for the first timeout
- Hard and soft configuration lock bits

4.6.8 External Watchdog (EWDG)

- Independent functional clock source
- Programmable time-out period
- Windowed refresh option
- Provides robust check that program flow is faster than expected
- Programmable window
- Refresh operation should be done within 63 peripheral bus clock cycles
- An output pad EWDG_OUT_b is used to indicate operation error
- An input pad EWDG_IN is used for external circuit to control EWDG_OUT_b output directly

4.7 Communication Interfaces

4.7.1 Flexible Controller Area Network (FlexCAN)

- Full implementation of the CAN FD protocol and CAN Specification 2.0, Part B
 - Standard data frames
 - Extended data frames
 - Zero to sixty-four bytes data length
 - Programmable bit rate
 - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Silicon-proven implementation passing ISO 16845-1:2016 CAN conformance tests
- Flexible mailboxes configurable to store 0 to 8, 16, 32, or 64 bytes data length

- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Legacy Rx FIFO with storage capacity for up to 6 CAN frames and automatic internal pointer handling with DMA support
- Full-featured Enhanced Rx FIFO with storage capacity for up to 32 CAN FD frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Flexible message buffers, totaling 128 message buffers of 8 bytes data length each, configurable as Rx or Tx
- Programmable clock source to the CAN Protocol Engine, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer, with an optional external time tick or high-resolution 32-bit on-chip timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the FlexCAN is synchronous with CAN bus
- CRC status for transmitted message
- Legacy Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Legacy Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 ID Filter Table elements
- Powerful Enhanced Rx FIFO ID filtering, capable of matching incoming IDs against either 64 extended or 128 standard ID filter elements with three filtering schemes: mask + filter, range, and two filters without mask
- 100% backward compatibility with previous FlexCAN version
- Support in low power modes: Deepsleep mode and Standby mode

4.7.2 Universal Asynchronous Receiver/Transmitter (UART)

- Support LIN break send and detect
- Transmit/Receive FIFO
- Support Transmit/Receive via DMA
- Baudrate setting
- 1-bit or 2-bit STOP size
- 7-bit, 8-bit, 9-bit or 10-bit frame size
- Transmit/Receive polarity setting
- Receive data match

- Line idle, address match wakeup
- Support transmit/receive line switch
- Support hardware flow control (CTS/RTS)
- Support single wire mode

4.7.3 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration
- Configurable frame size
- Transmit/Receive FIFO
- Support Transmit/Receive via DMA
- Support Standard/Dual/Quad SPI mode
- Support I2S standard transfer
- Support Master and Slave mode
- Support common PCS output for monitor

4.7.4 Inter-Integrated Circuit (I2C)

- Support standard, fast, fast plus, high speed and ultra fast mode
- Support 7-bit/10-bit address mode with master and slave
- Support SMBus mode
- Support multi-master arbitration and synchronization
- Support master and slave clock stretching
- Transmit/Receive FIFO (master only)
- Digital filter on both SCL and SDA pins
- Support transmit/receive data transfer via DMA

4.8 Human Machine Interface

4.8.1 General Purpose Input/Output (GPIO)

- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- Inversion for data inputs
- Interrupt flag and enable registers for each pin
- Support for edge sensitive (rising, falling, both) or level sensitive (low, high)
- Asynchronous wake-up in low-power modes
- Pin interrupt is functional in all digital pin muxing modes
- Support getting state of the port in all digital pin muxing modes

4.8.2 Port Controller (PCTRL)

- Individual pull control fields with pullup, pulldown, and pull-disable support
- Individual input passive filter field supporting enable and disable of the individual input passive filter on selected pins

- Individual drive strength field supporting low or high drive strength on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to 6 chip-specific digital functions
- Individual digital filter for data inputs
- Output Compare(readback) function enable on selected pins with digital filter
- Individual lock function to avoid misoperation

5 Ordering Information

The following chips are available for ordering.

Table 1: Ordering Information

Product	Memory			Package		IO and eADC channel		Communication
Part number	PFlash	DFlash	RAM	Pin count	Package	GPIOs (Normal)	eADC channels	FlexCAN
YTM32B1MD24H0MLLT	512KB	64KB	64KB	100	LQFP	88	32	3
YTM32B1MD24H0MLHT	512KB	64KB	64KB	64	LQFP	57	27	3
YTM32B1MD24H0MLFT	512KB	64KB	64KB	48	LQFP	42	20	3

5.1 Part Number Information

Table 2: Part Number Field Description

Field	Description	Values							
YTM	Product Status	YTM: Qualified PTM: Prototype							
32	MCU Type	32: 32-bit							
B	Product Line	B: General D: Dashboard P: Powertrain V: Vision N: Network Z: High voltage, integrity							
1	Generation	1st generation production							
Mx	Level	Product Line							
		B	Hx: High end Mx: Middle end Lx: Low end						
		Z	Mx: Motor+LIN-PHY Lx: LIN-PHY Cx: CAN-PHY Tx: Touch-sensor Dx: LED Driver						
2	Major Revision	1st revision							
4	Memory Size		0	1	2	3	4	5	6
		Z	-	-	-	32K	48K	64K	128K
		H	1M	2M	4M	6M	8M	12M	16M
		M	-	-	128K	256K	512K	1M	2M
		L	-	-	-	32K	64K	128K	256K
H0	Reserved	Reserved							
M	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C							
		Pins			LQFP	QFN	TSSOP	BGA	

Table 2 continued from previous page

Field	Description	Values					
LL	Package	8	-	-	TB	-	-
		10	-	-	TC	-	-
		12	-	-	TD	-	-
		14	-	-	TE	-	-
		16	-	-	TF	-	-
		20	-	-	TH	-	-
		24	-	FK	-	-	-
		32	LE	FM	-	-	-
		48	LF	FN	-	-	-
		64	LH	FO	-	-	-
		100	LL	-	-	MH	-
		144	LQ	-	-	-	-
		176	LU	-	-	-	-
		208	-	-	-	MK	-
		257	-	-	-	MM	-
		289	-	-	-	MQ	-
		320	-	-	-	MR	-
		373	-	-	-	MS	-
		416	-	-	-	MT	-
		516	-	-	-	MV	-
None	Optional Mode	S: Single end mode D: Differential mode I: ISELED C: Cost Optimization X: ISELED and Cost Optimization					
T ¹	Packing	T: Trays/Tubes R: Tape and Reel					

1. The chip mark doesn't contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
T _A M-Grade Part	Ambient temperature under bias	-40	-	125	°C
T _J M-Grade Part	Junction temperature under bias	-40	-	150	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Typ.	Max.	Notes
MSL	Moisture sensitivity level	–	3	–	1

NOTE:

- Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- Storage conditions are formulated in accordance with MSL3 standards. For specific requirements, refer to the instructions on the aluminum foil packaging bag. Chip storage shall meet the following: temperature < 40°C, humidity < 90% RH, storage period 24 months.

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	-500	500	V	
	Corner pins only	-750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	-100	100	mA	3
	Latch-up current at ambient temperature of 25 °C	-200	200	mA	

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

6.2 DC Characteristics

6.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	-0.3	5.8 ¹	V	
I_{VDD}	Maximum current into V_{DD}	–	150	mA	
V_{IO}	Digital/Analog IO Input voltage	-0.3	$V_{DD} + 0.3$	V	
I_O	Instantaneous maximum current of single pin	-25	25	mA	
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V	

1. 60 seconds lifetime - No restrictions i.e. the part is not held in reset and can switch.
- 10 hours lifetime - The part is held in reset by an external circuit i.e. the part cannot switch.

NOTE:

- The maximum ratings are the limits to which the device can be subjected without permanently damaging the device.
- The device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2.2 Voltage and Current Operating Requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.97	5.5	V	
V_{DDA}	Analog supply voltage	2.97	V_{DD}	V	
V_{REFH}	Reference voltage	2.97	V_{DDA}	V	
$V_{DD} - V_{DDA}$	V_{DD} to V_{DDA} differential voltage	-0.1	0.1	V	
I_{ICIO}^1	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-1	1	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of positive rejection currents of 16 contiguous pins	—	15	mA	
T_{ramp}	MCU supply ramp rate	5 V/100ms	100 V/ms	—	

1. All pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than $V_{SS} - 0.3V$ or greater than $V_{DD} + 0.3V$, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{SS} - 0.3V - V_{IN}) / |I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R = [V_{IN} - (V_{DD} + 0.3V)] / |I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.

6.2.3 DC Electrical Specifications at 3.3V

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	2.97	3.3	4.0	V	
V_{ih}	Input buffer high voltage	$0.7 * V_{DD}$	—	$V_{DD} + 0.3$	V	
V_{il}	Input buffer low voltage	$V_{SS} - 0.3$	—	$0.3 * V_{DD}$	V	
V_{hys}	Input buffer hysteresis	$0.06 * V_{DD}$	—	—	V	
I_{oh}	Normal drive I/O current source capability measured when pad = ($V_{DD} - 0.8V$)	5	12	—	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	5	15	—	mA	
I_{oh}	High drive I/O current source capability measured when pad = ($V_{DD} - 0.8V$)	10	24	—	mA	
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	10	24	—	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	—	50	500	nA	

Table 8 continued from previous page

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
	Hi-Z (Off state) leakage current (per pin) @125°C	–	100	500	nA	
V _{OH}	Output high voltage					
	Normal drive pad (2.97V ≤ V _{DD} ≤ 4.0V, I _{OH} = -2.8mA)	V _{DD} - 0.8	–	V _{DD}	V	
V _{OL}	Output low voltage					
	Normal drive pad (2.97V ≤ V _{DD} ≤ 4.0V, I _{OL} = -2.8mA)	V _{SS}	–	0.8	V	
I _{OLT}	Output low current total for all ports	–	–	50	mA	
I _{IN}	Input leakage current (per pin) for full temperature range					
	Normal pins	–	–	0.5	μA	
	High drive pins	–	–	0.5	μA	
R _{PU}	Internal pull-up resistors	15	–	100	kΩ	
R _{PD}	Internal pull-down resistors	15	–	105	kΩ	

6.2.4 DC Electrical Specifications at 5.0V

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V _{DD}	I/O supply voltage	4	5	5.5	V	
V _{ih}	Input buffer high voltage	0.65 * V _{DD}	–	V _{DD} + 0.3	V	
V _{il}	Input buffer low voltage	V _{SS} - 0.3	–	0.35 * V _{DD}	V	
V _{hys}	Input buffer hysteresis	0.06 * V _{DD}	–	–	V	
I _{oh}	Normal drive I/O current source capability measured when pad = (V _{DD} - 0.8V)	10	17	–	mA	
I _{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	10	20	–	mA	
I _{oh}	High drive I/O current source capability measured when pad = (V _{DD} - 0.8V)	10	30	–	mA	
I _{ol}	High drive I/O current sink capability measured when pad = 0.8V	10	35	–	mA	
I _{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	50	500	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	100	500	nA	
V _{OH}	Output high voltage					
	Normal drive pad (2.97V ≤ V _{DD} ≤ 4.0V, I _{OH} = -2.8mA)	V _{DD} - 0.8	–	V _{DD}	V	

Table 9 continued from previous page

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{OL}	Output low voltage					
	Normal drive pad ($2.97V \leq V_{DD} \leq 4.0V$, $I_{OL} = -2.8mA$)	V_{SS}	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	50	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	Normal pins	–	–	0.5	μA	
	High drive pins	–	–	0.5	μA	
R_{PU}	Internal pull-up resistors	15	–	100	$k\Omega$	
R_{PD}	Internal pull-down resistors	15	–	100	$k\Omega$	

6.2.5 Power and Ground Pins

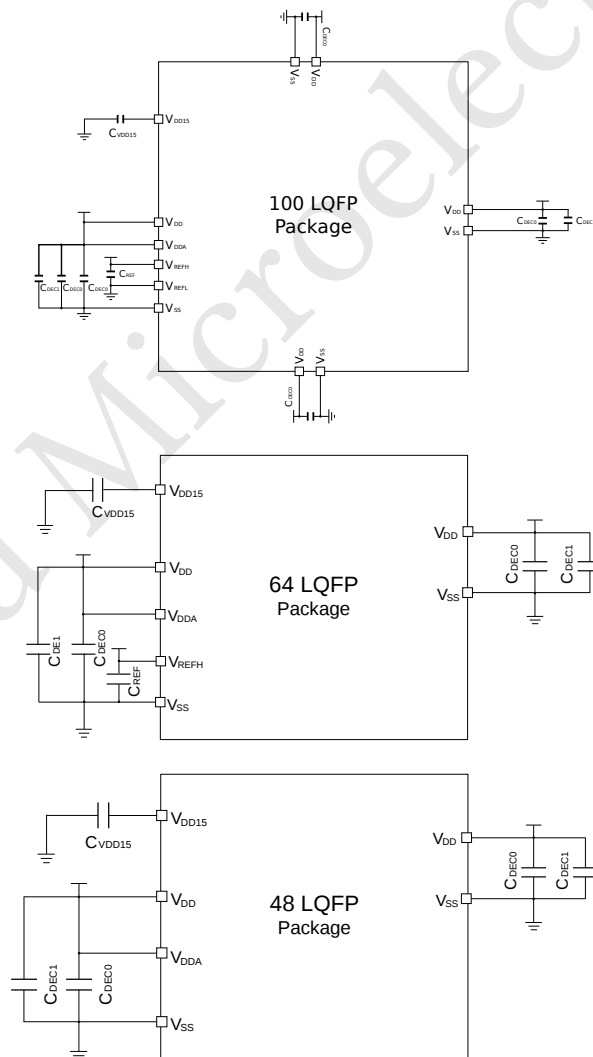


Figure 2: Pinout Decoupling

Symbol	Description	Min.	Typ.	Max.	Unit
C _{REF} ^{1,2,3}	eADC reference high decoupling capacitance	50	100	200	nF
C _{DECO} ^{2,3,4}	Recommended decoupling capacitance	2.2	4.7	20	μF
C _{DEC1} ^{2,3,4}	Recommended decoupling capacitance	50	100	200	nF
C _{VDD15}	Recommended decoupling capacitance	1	2.2	2.2	μF

1. For improved performance, it is recommended to use 10 μF, 0.1 μF and 1nF capacitors in parallel.
2. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
3. All decoupling capacitors must be low ESR ceramic capacitors(for example X7R type).
4. The requirement and value of C_{DEC} will be decided by the device application requirement.

6.2.6 LVR and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{LVR}	Rising and falling V _{DD} LVR detect voltage	–	2.5	2.7	V	
V _{LVD}	Falling low-voltage threshold(LVDCFG=5)	2.97	3.1	3.4	V	
	Falling low-voltage threshold(LVDCFG=10)	3.7	4.0	4.5	V	
V _{LVD_HYST}	LVD hysteresis(LVD5VHYS=01b)	-2	–	2	%	1
	LVD hysteresis(LVD5VHYS=10b)	-4.2	–	4.2	%	1
	LVD hysteresis(LVD5VHYS=11b)	-8.4	–	8.4	%	1
V _{bg}	Bandgap voltage reference	0.96	1.0	1.04	V	
V _{DD15}	MCU VDD15 LDO output voltage	1.46	1.62	1.78	V	

1. All data presented are simulation values.

6.2.7 Power Mode Transition Operating Behaviors

Description	System clock	Core, bus frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	FIRC	48MHz/24MHz	–	2μs	–
DEEPSLEEP -> ACTIVE	FIRC	48MHz/24MHz	–	36μs	–
STANDBY -> ACTIVE	FIRC	48MHz/24MHz	–	200μs	–
T _{POR}	FIRC(reset value)	48MHz/24MHz	–	500μs	–

6.2.8 Power Consumption

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
ACTIVE	I _{DD_ACTIVE}	PLL	Running while(1) loop in flash, all peripheral clock enabled. core @80MHz, bus @40MHz V _{DD} =5V	25 °C	–	29	50	mA
				125 °C	–	33	60	mA

Table 13 continued from previous page

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
			Running while(1) loop in flash, all peripheral clock disabled. core @80MHz, bus @40MHz $V_{DD}=5V$	25 °C	–	19	45	mA
				125 °C	–	22	55	mA
SLEEP	I_{DD_SLEEP}	PLL	Sleep mode current, $V_{DD}=5V$	$\leq 25\text{ °C}$	–	7.5	15	mA
				125 °C	–	9.5	20	mA
DEEPSLEEP	$I_{DD_DEEPSLEEP}$	–	Deepsleep mode current, $V_{DD}=5V$ SIRC=1	$\leq 25\text{ °C}$	–	160	240	μA
				125 °C	–	250	420	μA
			Deepsleep mode current, $V_{DD}=5V$ SIRC=0	$\leq 25\text{ °C}$	–	135	210	μA
				125 °C	–	230	380	μA
STANDBY	$I_{DD_STANDBY}$	–	Standby mode current, $V_{DD}=5V$ SIRC=1	$\leq 25\text{ °C}$	–	35	65	μA
				125 °C	–	120	225	μA
			Standby mode current, $V_{DD}=5V$ SIRC=0	$\leq 25\text{ °C}$	–	7	25	μA
				125 °C	–	95	185	μA

6.2.9 Power Sequence

6.2.9.1 Power Up Sequence

Hardwares must follow sequence below to ensure that the chip is powered up properly.

1. VDD must be powered up first.
2. VDDA must be powered up later than or at the same time as VDD.
3. VREFH must be powered up later than or at the same time as VDDA.

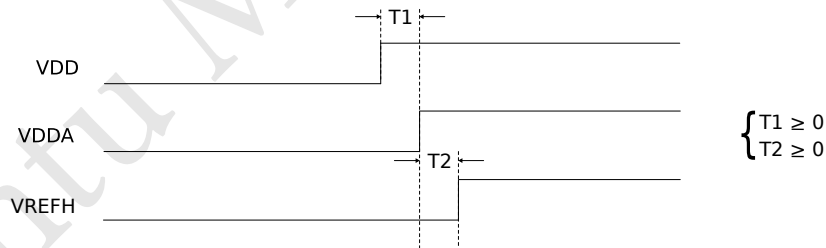


Figure 3: Power Sequence

6.2.9.2 MCU Power Supply Ramp Rate

During the power-up sequence of MCU, it is critical that the power supply maintains a ramp-rate within the specified range, starting from V_{DD_OFF} at 0.1V and rising to the MCU's operational voltage level (V_{DD}). Failure to comply with this specification may result in unintended behavior, operational stagnation or even damage to the MCU.

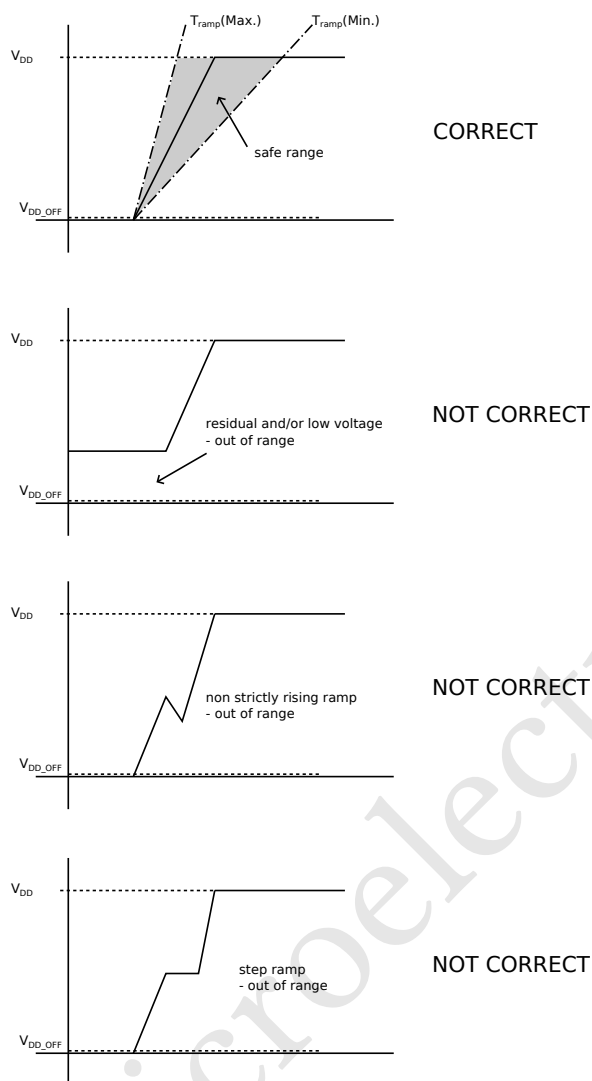
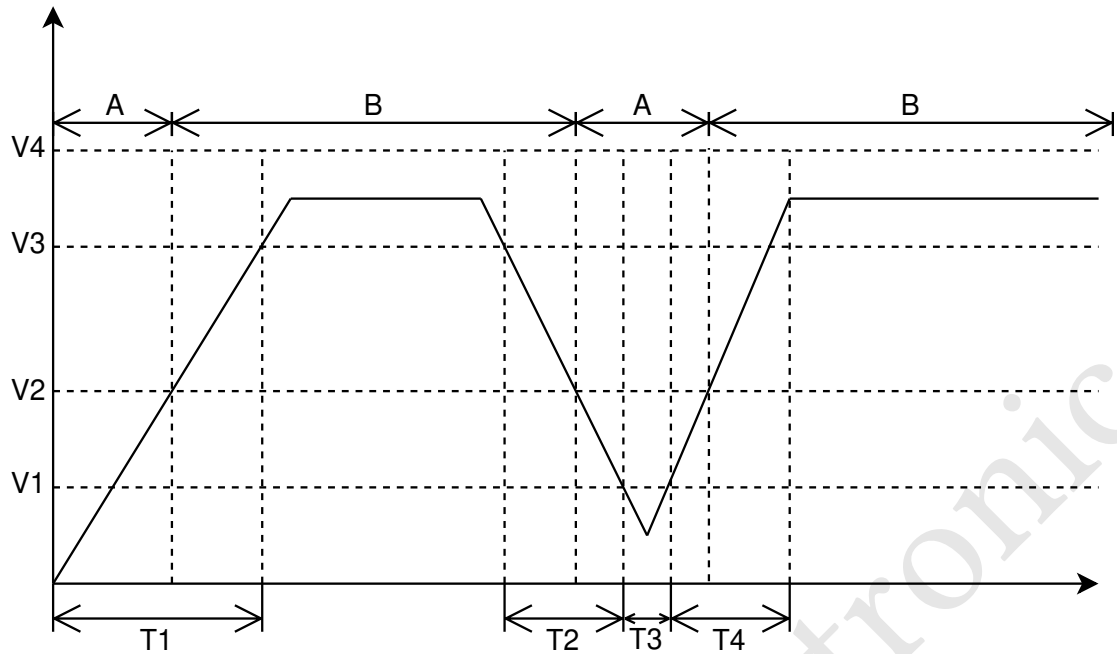


Figure 4: Power Supply Ramp Rate

6.2.9.3 Power Up Requirements

It is necessary to ensure that V_{DD} meets the following timing during the power-up process of YTM32B1MD2x.



A : There is no guarantee of proper functionality when the MCU is in uncertain status.

B : The MCU operates normally.

Figure 5: Power Up Requirements

Symbol	Name	Description	Unit (V)
V1	Restart threshold voltage	When restarting the MCU, VDD should keep below V1 for a period of T3.	1
V2	Minimum MCU operating voltage	The MCU starts working when the power supply reaches V2.	2.5
V3	Lower voltage limit of MCU operating normally	Minimum operating voltage for normal MCU operation and interaction with peripherals.	2.97
V4	Upper voltage limit of MCU operating normally	Maximum operating voltage for normal MCU operation and interaction with peripherals	5.5

Symbol	Name	Description	Requirement
T1	Power up time	Rising time of MCU VDD from 0V to V3	$10\ \mu\text{s} < T1 < 50\text{ms}$
T2	Power down time	Drop time of MCU VDD from V3 to V1 during the MCU restart/power down process	$10\ \mu\text{s} < T2 < 500\text{ms}$
T3	Restart threshold voltage retain time	Minimum duration of MCU VDD below V1, when restarting MCU	$T3 > 100\ \mu\text{s}$
T4	Restart power up time	Rising time of MCU VDD normal operation from V1 to V3	$10\ \mu\text{s} < T4 < 50\text{ms}$

NOTE: The power-up process needs to be restarted if a VDD voltage drop occurs during the T1~T4 power-up process before the VDD voltage reaches the V2 voltage. Restarting the power-up of MCU needs to ensure that the voltage of VDD continues to drop below V1 and remains there for T3 time.

6.2.10 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance.

6.3 AC Characteristics

6.3.1 Power Supply Fluctuation Requirements

1. The power supply fluctuation must be maintained within $\pm 10\%$ of the power supply voltage, and the fluctuation frequency should not exceed 100 KHz.
2. The maximum power supply fluctuation should not exceed $\pm 20\%$ of the power supply voltage, and in this case, the fluctuation frequency should be less than 30 KHz.
3. Power supply fluctuations exceeding the above requirements may cause chip abnormalities and require a power-up process according to the requirements outlined in [Power Up Requirements](#).

6.3.2 Device Clock Specifications

Symbol	Description	Min.	Typ.	Unit	Notes
F_{core}	System and core clock	–	80	MHz	
F_{bus}	Fast bus clock	–	80	MHz	
	Slow bus clock	–	40	MHz	

6.3.3 I/O Electrical Characteristics

6.3.3.1 AC Electrical Characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and the rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

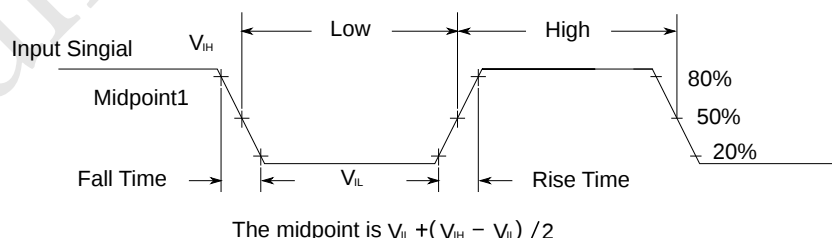


Figure 6: Input Signal Measurement Reference

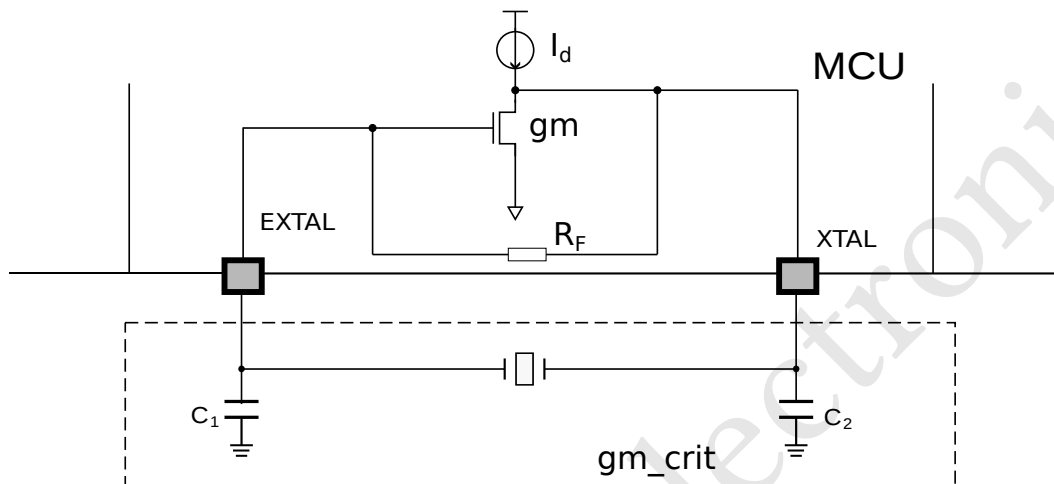
All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L = 30\text{pF}$ loads
- Normal drive strength

6.4 Peripheral Operating Requirements and Behaviors

6.4.1 FXOSC(4~40MHz) Characteristics

The following diagram is Fast Crystal OSC circuit.



■ The internal circuitry of the chip utilizes an I_d current source as the load for the amplifier circuit, with an NMOS transistor serving as the amplifying transistor. When the gain (g_m) of the amplifying transistor is greater than the intrinsic gain (g_{m_crit}) of the external crystal oscillator, theoretically, the crystal oscillator will start to oscillate. Generally, it is required that $g_m > 5 \cdot g_{m_crit}$.

■ R_F provides the DC bias point for the input terminal of the amplifying transistor.

Figure 7: FXOSC Diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.97	–	5.5	V	
V_{IH}	Input high voltage – EXTAL pin in external clock mode, $V_{DD}=5\text{V}$	$0.7 \cdot V_{DD}$	–	V_{DD}	V	
	Input high voltage – EXTAL pin in external clock mode, $V_{DD}=3.3\text{V}$	$0.7 \cdot V_{DD}$	–	V_{DD}	V	
V_{IL}	Input low voltage – EXTAL pin in external clock mode, $V_{DD}=5\text{V}$	V_{SS}	–	$0.3 \cdot V_{DD}$	V	
	Input low voltage – EXTAL pin in external clock mode, $V_{DD}=3.3\text{V}$	V_{SS}	–	$0.3 \cdot V_{DD}$	V	
$T_{FXOSCSU}$	FXOSC startup time (40MHz oscillator)	–	1	–	ms	
D_{FXOSC}	Duty of FXOSC (40MHz oscillator)	40	–	60	%	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	FXOSC internal feedback resistor	–	500	–	k Ω	
V_{PP}	Peak-to-peak amplitude of oscillation (40MHz oscillator) (alc_pd=0)	0.75	–	4.1	V	

1. Crystal oscillator circuit provides stable oscillations when $gm > 5 * gm_{crit}$. The gm_{crit} is defined as:
 $gm_{crit} = 4 * (ESR + R_S) * (2\pi F)^2 * (C_0 + C_L)^2$

where:

- gm is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- R_S is the series resistance connected between XTAL pin and external crystal for current limitation
- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_S + [C_1 * C_2 / (C_1 + C_2)]$
- C_S is stray or parasitic capacitance on the pin due to any PCB traces
- C_1 and C_2 are external load capacitances on EXTAL and XTAL pins.

Table 18: Startup Time - Gain Selection for gm of 40MHz Crystal Oscillator Circuits (Simulation)

Gain Setting	gm (at statup)			Unit
	Min.	Typ.	Max.	
0			0	mS
1	2.04	2.78	3.52	mS
2	4.06	5.54	7.01	mS
3	6.07	8.27	10.46	mS
4	8.07	10.98	13.88	mS
5	10.07	13.64	17.21	mS
6	12.03	16.29	20.54	mS
7	13.99	18.91	23.82	mS

6.4.2 FIRC(48MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{FIRC}	Fast internal reference frequency	–	48	–	MHz	
ACC_{FIRC}	FIRC frequency accuracy, factory trimmed, 25°C	-3	–	3	%	
	FIRC frequency accuracy, factory trimmed, -40°C – 125°C	-5	–	5	%	
I_{FIRC}	FIRC operating current	–	260	–	μA	
$T_{Startup}$	Startup time	–		20	μs	

NOTE:

- For CAN communication, high-precision clock sources (e.g., FXOSC, PLL) must be used to comply with ISO 11898-1 standard; FIRC is not recommended for direct use as the PE clock of FlexCAN.
- For LIN/UART communication, it is recommended to use high-precision clock sources (e.g., FXOSC, PLL); if FIRC is used, evaluation must be conducted on frequency differences between chips, temperature effects, and frequency deviations of other devices in LIN/UART network.

- For applications with high requirements on the absolute frequency of the clock (e.g., PWM output, timing tasks), evaluation must be conducted on frequency differences between FIRC and SIRC among different chips and their temperature effects.

6.4.3 SIRC(2MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F _{SIRC}	Slow internal reference frequency	–	2	–	MHz	
ACC _{SIRC}	SIRC frequency accuracy, factory trimmed, 25 °C	-5	–	5	%	
	SIRC frequency accuracy, factory trimmed, –40 °C – 125 °C	-8	–	8	%	
I _{SIRC}	SIRC operating current	–	15	–	μA	
T _{Startup}	Startup time	–	20	50	μs	

NOTE:

- For CAN communication, high-precision clock sources (e.g., FXOSC, PLL) must be used to comply with ISO 11898-1 standard; FIRC is not recommended for direct use as the PE clock of FlexCAN.
- For LIN/UART communication, it is recommended to use high-precision clock sources (e.g., FXOSC, PLL); if FIRC is used, evaluation must be conducted on frequency differences between chips, temperature effects, and frequency deviations of other devices in LIN/UART network.
- For applications with high requirements on the absolute frequency of the clock (e.g., PWM output, timing tasks), evaluation must be conducted on frequency differences between FIRC and SIRC among different chips and their temperature effects.

6.4.4 PLL Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F _{ref}	PLL reference frequency range	4	–	48	MHz	
F _{input}	PLL input frequency	4	–	48	MHz	5
F _{vco}	VCO frequency	120	160	160	MHz	
F _{out}	Out frequency	60	80	80	MHz	1, 4
N _{pre}	Reference clock predivider	0	–	15		2
N _{div}	VCO feedback divider	2	–	63		3
T _{lock}	PLL lock time	–	5120*T _{input}	–		5

1. PLL OUT divider is 2, $F_{out} = F_{vco}/2$

2. PLL clock pre-divider is from 1 to 16. If need to re-configure. It is recommended to switch to other clock source, then disable PLL, and configure PLL predivider, switch to PLL, and enable it finally.

3. PLL clock feedback divider is from 2 to 63. It is recommended to switch to other clock source, then disable PLL, and configure PLL predivider, switch to PLL, and enable it finally.

4. $F_{input} = \frac{F_{ref}}{N_{pre}+1}$

5. T_{input} represents the PLL input period.

6.4.5 LPO(32KHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{LPO}	Low power oscillator frequency	–	32	–	KHz	
ACC_{LPO}	LPO frequency accuracy, factory trimmed, 25 °C	-10	–	10	%	
	LPO frequency accuracy, factory trimmed, –40 °C – 125 °C	-20	–	20	%	

6.4.6 eADC Characteristics

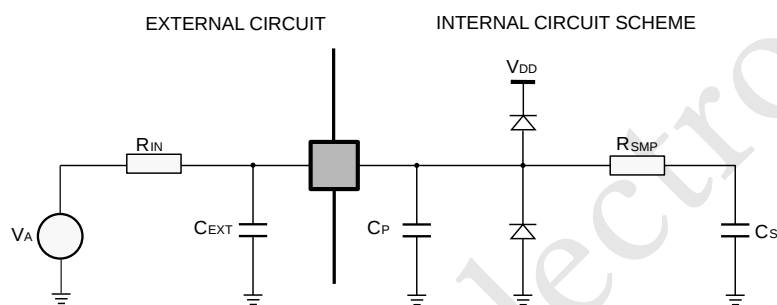


Figure 8: eADC Circuit

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage		2.97	5.0	5.5	V	
ΔV_{DDA}	$V_{DD} - V_{DDA}$		0	–	100	mV	
V_{REFH}	Reference voltage		2.97	–	V_{DDA}	V	
I_{REFH}	Reference current		–	–	800	μA	
V_{IN}	Input voltage		V_{SS}	–	V_{REFH}	V	
R_{SMP}	Sampling switch impedance		–	–	1.5	k Ω	
C_{EXT}	External capacitance		50	–	–	nF	
C_P	Pin Capacitance		–	3	–	pF	
C_S	Sampling capacitance		–	6	7	pF	

Symbol	Description	Test condition ¹	Min.	Typ.	Max.	Unit	Notes
$T_{STARTUP}$	Analog startup time		5	–	–	μs	
T_{SAMPLE}	Sampling time	–	200	–	2000	ns	
T_{sample_TS}	Tempensor sampling time		500	–	2000	ns	

1. Theses parameters of this table can be configured by register, please refer to Reference Manual for details.

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
DNL	Differential nonlinear	12-bit resolution	–	±1	–	LSB
INL	Integer nonlinear	12-bit resolution	–	±2	–	LSB
ACC _{tempS}	Temperature sensor accuracy		-10		10	°C
K ¹	Slope of temperature and voltage curve	eADC sampling frequency @ 500kHz		637		
F _{eADC} ²	eADC conversion clock		2		16	MHz

1. $T = C - K \cdot V$, see Reference Manual for details.

2. eADC conversion clock = eADC function clock / [(ipc_divider + 1) * (eadc_clock_div + 1)]

6.4.7 ACMP Characteristics

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V _{ACMP} ¹	Analog supply voltage		2.97	5.0	5.5	V	
I _{ACMP}	Analog supply current with no DAC buffer		–	20	50	μA	Low Power Mode
V _{INOFFSET}	Analog input offset voltage		–	–	14	mV	MC Simulation
V _{IN}	Analog input voltage		V _{SS}	–	V _{DDA}	V	
V _{HYST0}	Analog comparator hysteresis 0		12	20	45	mV	
V _{HYST1}	Analog comparator hysteresis 1		24	40	85	mV	
V _{HYST2}	Analog comparator hysteresis 2		36	60	130	mV	
DAC _{DNL}	Differential nonlinear		–	±1	–	LSB	
R _{load_dacbuf}	DAC buffer resistance loading ability		10	–	–	kΩ	
C _{load_dacbuf}	DAC buffer capacitance loading ability		–	–	25	pF	

1. This connects to VDD.

6.4.8 SPI Characteristics¹

Num.	Symbol	Description	Conditions	Min.	Max.	Unit
	f _{func} ²	Functional frequency	Slave	–	80	MHz
			Master	–	80	MHz
			Master Loopback ⁴	–	80	MHz
1	f _{op}	Frequency of operation	Slave	–	10	MHz
			Master	–	10	MHz
			Master Loopback ⁴	–	20	MHz
2	t _{SCK}	SCK period	Slave	100	–	ns

Table 27 continued from previous page

Num.	Symbol	Description	Conditions	Min.	Max.	Unit
			Master	100	–	ns
			Master Loopback ⁴	50	–	ns
3	t _{PCSSCK} ⁵	PCS to SCK delay	Slave	–	–	ns
			Master	(PCSSCK+1) * t _{delay} ³	–	ns
			Master Loopback ⁴	(PCSSCK+1) * t _{delay} ³	–	ns
4	t _{SCKPCS} ⁶	After SCK delay	Slave	–	–	ns
			Master	(SCKPCS+1) * t _{delay} ³	–	ns
			Master Loopback ⁴	(SCKPCS+1) * t _{delay} ³	–	ns
5	t _{WSCK} ⁷	Clock (SCK) high or low time	Slave	t _{SCK} /2 - 1	t _{SCK} /2 + 1	ns
			Master	t _{SCK} /2 - 1	t _{SCK} /2 + 1	ns
			Master Loopback ⁴	t _{SCK} /2 - 1	t _{SCK} /2 + 1	ns
6	t _{setup}	Data setup time (inputs)	Slave	12.5	–	ns
			Master	25	–	ns
			Master Loopback ⁴	10	–	ns
7	t _{holdin}	Data hold time (inputs)	Slave	0	–	ns
			Master	0	–	ns
			Master Loopback ⁴	0	–	ns
8	t _{valid}	Data valid (after SCK edge)	Slave	–	25	ns
			Master	–	15	ns
			Master Loopback ⁴	–	15	ns
9	t _{holdout}	Data hold time (outputs)	Slave	0	–	ns
			Master	0	–	ns
			Master Loopback ⁴	0	–	ns
10	t _{RI/FI}	Rise/Fall time input	Slave	–	1	ns
			Master	–	1	ns
			Master Loopback ⁴	–	1	ns
11	t _{RO/FO}	Rise/Fall time output	Slave	–	5	ns
			Master	–	5	ns
			Master Loopback ⁴	–	5	ns

1. The trace length for the SCK pad should be kept as short as possible when used in Master loopback mode, and it does not support off-board communication.

2. f_{func} = SPI functional clock, which is generated from IPC.

3. t_{delay} = (1/f_{op}) * 2^{TXCFG[PRESALE]}.

4. Master Loopback mode - In this mode SCK clock is delayed for sampling the input data which is enabled by setting SPI_CTRL[SPDEN] bit as 1.

5. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of SPI delay clock, where PCSSCK ranges from 0 to 255.

6. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of SPI delay clock, where SCKPCS ranges from 0 to 255.

7. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.

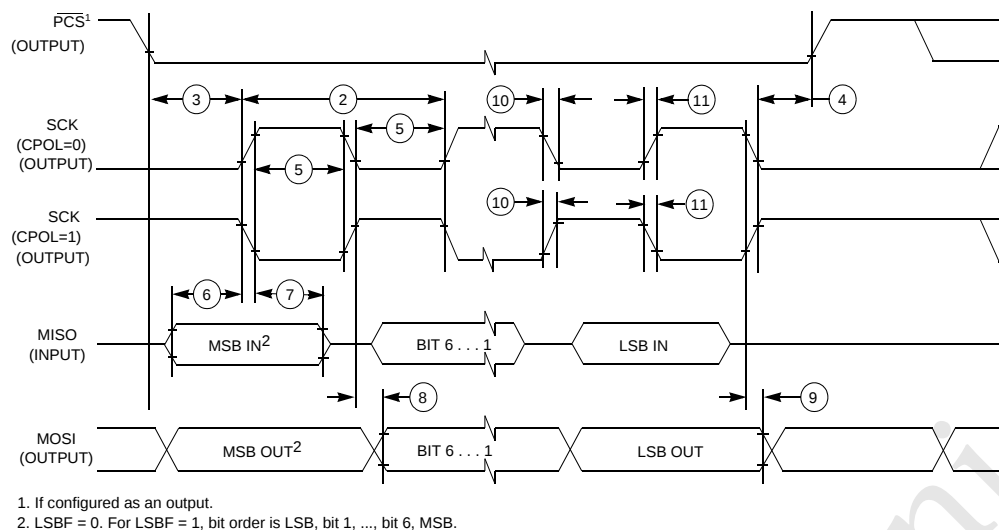


Figure 9: SPI Master Mode Timing (CHPA=0)

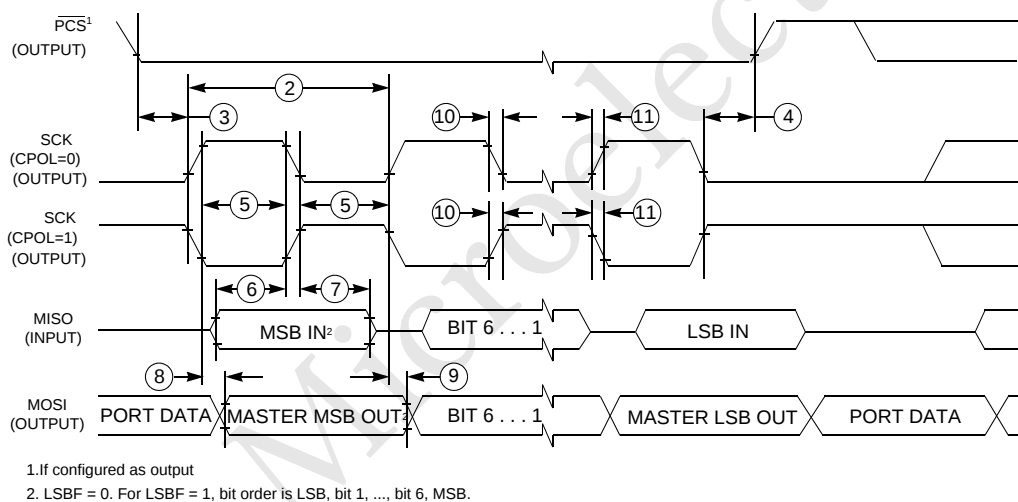
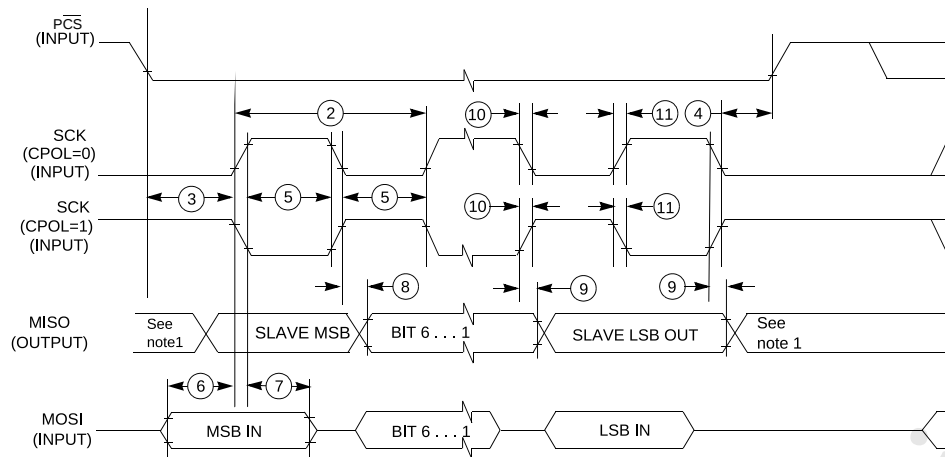


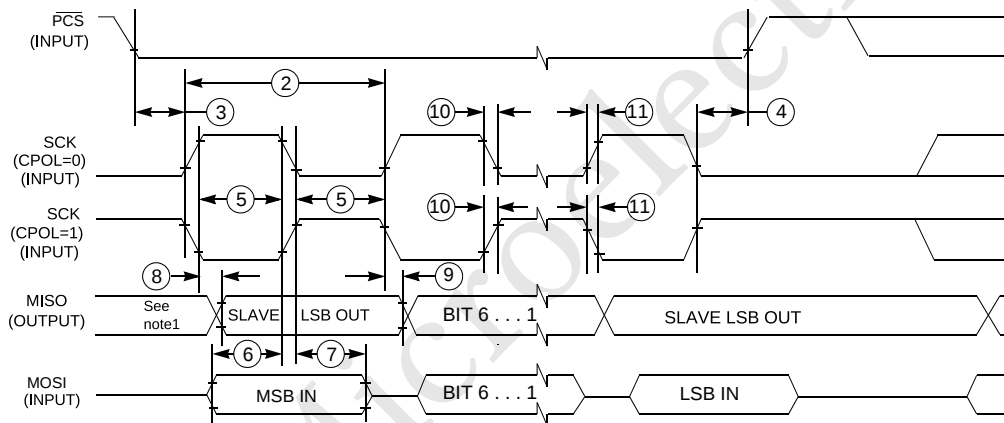
Figure 10: SPI Master Mode Timing (CHPA=1)



Notes:

1. The bus is driven but may not be equal to the valid serial data being sent.

Figure 11: SPI Slave Mode Timing (CHPA=0)



Notes:

1. The bus is driven but may not be equal to the valid serial data being sent.

Figure 12: SPI Slave Mode Timing (CHPA=1)

6.4.9 NVM Specifications

6.4.9.1 Flash Command Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T_{pgm32}	Program 32 bits execution time	158.7	–	164.7	μs	
T_{pgm8}	Program 8 bits execution time	139.7	–	141.2	μs	DFlash only
T_{sector_erase}	Sector erase execution time	2	–	3	ms	
T_{block_erase}	Block erase execution time	30	–	40	ms	

NOTE: PFlash and DFlash have the same command timing specifications of T_{pgm32} , T_{sector_erase} , and T_{block_erase} .

6.4.9.2 Reliability Specifications

Symbol	Description	Min.	Max.	Unit	Notes
t_{nmretp}	Data retention @25°C	20	–	years	
t_{nmcyep}	Cycling endurance	100K	–	cycles	

6.4.10 Debug Module Electrical

6.4.10.1 SWD Electrical Specifications

Table 30: SWD Full Voltage Range Electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

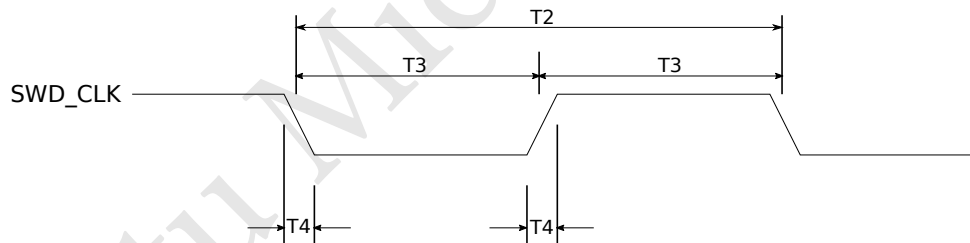


Figure 13: SWD Clock Timing

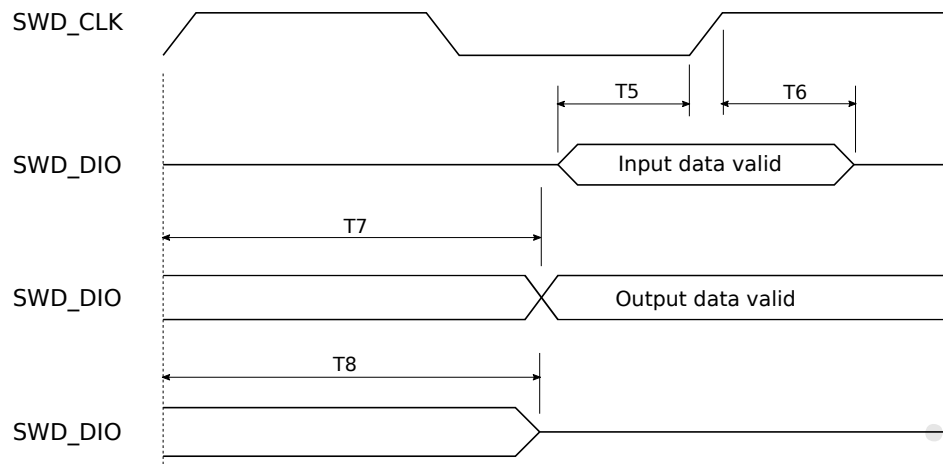


Figure 14: SWD Data Timing

6.4.10.2 JTAG Electrical Specifications

Table 31: JTAG Electrical Specifications

Symbol	Description	Active				Unit
		5.0V IO		3.3V IO		
		Min.	Max.	Min.	Max.	
J1	TCLK frequency					MHz
	Boundary Scan	–	20	–	20	
	JTAG	–	20	–	20	
J2	TCLK cycle period	1/J1	–	1/J1	–	ns
J3	TCLK clock pulse width					ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG					
J4	TCLK rise and fall times	–	1	–	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	–	5	–	ns
J6	Boundary scan input data hold time after TCLK rise	5	–	5	–	ns
J7	TCLK low to boundary scan output data valid	–	28	–	32	ns
J8	TCLK low to boundary scan output data invalid	0	–	0	–	ns
J9	TCLK low to boundary scan output high-Z	–	28	–	32	ns
J10	TMS, TDI input data setup time to TCLK rise	3	–	3	–	ns
J11	TMS, TDI input data hold time after TCLK rise	2	–	2	–	ns
J12	TCLK low to TDO data valid	–	28	–	32	ns
J13	TCLK low to TDO data invalid	0	–	0	–	ns
J14	TCLK low to TDO high-Z	–	28	–	28	ns

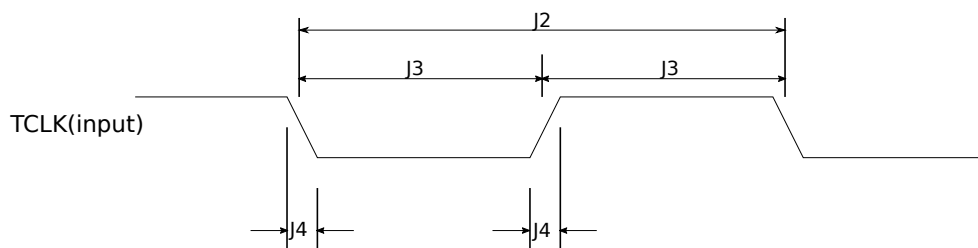


Figure 15: JTAG Clock Timing

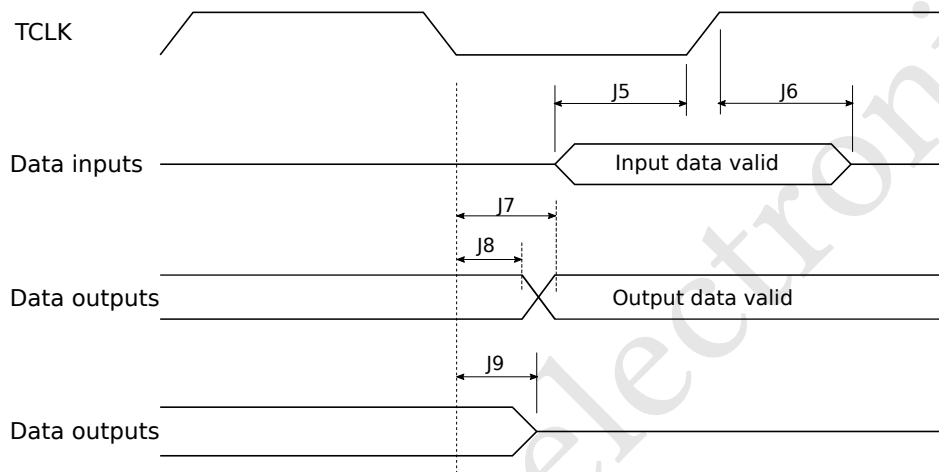


Figure 16: JTAG Data Timing

6.5 Thermal Attributes

Table 32: Thermal Characteristics

Package Family	Package Type	Thermal Resistance			Unit
		R _{JA}	R _{JC}	R _{JB}	
LQFP	LQFP48L	78	16	32	°C/W
	LQFP64L	65	13	30	°C/W
	LQFP100L	57	13	28	°C/W

NOTE: Based on environmental simulation per JEDEC standards, the PCB is a JEDEC-compliant 2S2P board. Data in this table is for reference only.

7 Pinouts

7.1 IO Signal Description

The pinouts signal description is as follows:

Table 33: Pinmux Table

100LQFP	64LQFP	48LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1			PTE_16		PTE_16	UART1_RTS	SPI2_SIN	MPWM0_CH7			TMU_OUT7
2			PTE_15		PTE_15	UART1_CTS	SPI2_SCK	MPWM0_CH6			TMU_OUT6
3	1	1	VDD15	VDD15							
4	2	2	PTD_0		PTD_0	eTMR0_CH2	SPI1_SCK	MPWM0_CH0	I2C1_SDA		TMU_OUT1
5	3		PTE_11		PTE_11	SPI2_PCS0	lpTMR0_ALT1	MPWM0_CH5			TMU_OUT5
6	4		PTE_10		PTE_10	CFMU_CLKOUT	SPI2_PCS1	MPWM0_CH4			TMU_OUT4
7			PTE_13		PTE_13		SPI2_PCS2	eTMR0_FLT0			
8	5	3	PTE_5		PTE_5	TCLK_IN2	eTMR0_QD_PHA	MPWM0_CH3	CAN0_TX	I2C0_SCL	EWDG_IN
9	6	4	PTE_4		PTE_4	eTMR0_FLT0	eTMR0_QD_PHB	MPWM0_CH2	CAN0_RX	I2C0_SDA	EWDG_OUT_b
10	7	5	VDD	VDD							
11	8	6	VDDA	VDDA							
12	9		VREFH	VREFH							
13			VREFL	VREFL							
14	10	7	VSS	VSS							
15	11	8	PTB_7	EXTAL	PTB_7	I2C0_SCL		SPI0_SCK	UART2_TX		TMU_OUT2
16	12	9	PTB_6	XTAL	PTB_6	I2C0_SDA		SPI0_SIN	UART2_RX		TMU_OUT1
17			PTE_14		PTE_14	eTMR0_FLT1		eTMR1_FLT1			
18	13		PTB_3		PTB_3	eTMR0_FLT0	UART2_RTS	eTMR1_FLT0	SPI0_SOUT	TMU_IN6	ACMP0_OUT
19			PTE_12		PTE_12	eTMR0_FLT3	UART2_TX		SPI0_PCS0		
20			PTD_17		PTD_17	eTMR0_FLT2	UART2_RX	SPI0_PCS_COM			
21	14	10	PTD_16		PTD_16	eTMR0_CH1		SPI0_SIN	ACMP0_ACTIVE		
22	15	11	PTD_15		PTD_15	eTMR0_CH0		SPI0_SCK	RTC_CLKIN		
23	16	12	PTE_9		PTE_9	eTMR0_CH7	UART2_CTS	SPI0_PCS_COM			
24			PTD_14		PTD_14	MPWM0_CH5	UART1_TX	SPI1_PCS_COM			CFMU_CLKOUT
25			PTD_13		PTD_13	MPWM0_CH4	UART1_RX	SPI1_PCS_COM			RTC_CLKOUT
26	17	13	PTE_8	ACMP0_IN3	PTE_8	eTMR0_CH6			SPI0_PCS1		
27	18	14	PTB_5		PTB_5	eTMR0_CH5	SPI0_PCS1	SPI0_PCS0	CFMU_CLKOUT	TMU_IN0	
28	19	15	PTB_4		PTB_4	eTMR0_CH4	SPI0_SOUT			TMU_IN1	
29	20	16	PTC_3	eADC0_SE11/ACMP0_IN4	PTC_3	eTMR0_CH3	CAN0_TX	UART0_TX			
30	21	17	PTC_2	eADC0_SE10/ACMP0_IN5	PTC_2	eTMR0_CH2	CAN0_RX	UART0_RX			
31	22		PTD_7	ACMP0_IN6	PTD_7	UART2_TX	eTMR0_CH3	eTMR0_FLT3			
32	23		PTD_6	ACMP0_IN7	PTD_6	UART2_RX	eTMR0_CH2	eTMR0_FLT2			SPI0_PCS3
33	24	18	PTD_5		PTD_5	MPWM0_CH3	lpTMR0_ALT2	eTMR0_FLT1	CFMU_CLKOUT	TMU_IN7	SPI0_PCS1
34			PTD_12		PTD_12	MPWM0_CH2				UART2_RTS	
35			PTD_11		PTD_11	MPWM0_CH1	eTMR0_QD_PHA			UART2_CTS	
36			PTD_10		PTD_10	MPWM0_CH0	eTMR0_QD_PHB			CFMU_CLKOUT	
37			VSS	VSS							
38			VDD	VDD							
39	25	19	PTC_1	eADC0_SE9	PTC_1	eTMR0_CH1	SPI2_SOUT			eTMR1_CH7	
40	26		PTC_0	eADC0_SE8	PTC_0	eTMR0_CH0	SPI2_SIN			eTMR1_CH6	
41			PTD_9		PTD_9			eTMR0_FLT3		eTMR1_CH5	
42			PTD_8		PTD_8			eTMR0_FLT2		eTMR1_CH4	
43	27		PTC_17	eADC0_SE15	PTC_17	eTMR1_FLT3	CAN2_TX		MPWM0_CH1		
44	28	20	PTC_16	eADC0_SE14	PTC_16	eTMR1_FLT2	CAN2_RX		MPWM0_CH0		
45	29	21	PTC_15	eADC0_SE13	PTC_15	eTMR1_CH3	SPI2_SCK			TMU_IN8	
46	30	22	PTC_14	eADC0_SE12	PTC_14	eTMR1_CH2	SPI2_PCS0			TMU_IN9	
47	31	23	PTB_3	eADC0_SE7	PTB_3	eTMR1_CH1	SPI0_SIN	eTMR1_QD_PHA		TMU_IN2	
48	32	24	PTB_2	eADC0_SE6	PTB_2	eTMR1_CH0	SPI0_SCK	eTMR1_QD_PHB	RTC_CLKIN	TMU_IN3	
49			PTC_13		PTC_13	MPWM0_CH15	MPWM0_CH7	UART2_RTS			
50			PTC_12		PTC_12	MPWM0_CH14	MPWM0_CH6	UART2_CTS			
51			PTC_11		PTC_11	MPWM0_CH13		SPI2_PCS_COM		TMU_IN10	
52			PTC_10		PTC_10	MPWM0_CH12		SPI2_PCS_COM		TMU_IN11	
53	33	25	PTB_1	eADC0_SE5	PTB_1	UART0_TX	SPI0_SOUT	TCLK_IN0	CAN0_TX	lpTMR0_ALT1	
54	34	26	PTB_0	eADC0_SE4	PTB_0	UART0_RX	SPI0_PCS0	lpTMR0_ALT3	CAN0_RX		
55	35	27	PTC_9		PTC_9	UART1_TX	eTMR1_FLT1	eTMR0_FLT1		UART0_RTS	
56	36	28	PTC_8	DAC0_OUT	PTC_8	UART1_RX	eTMR1_FLT0			UART0_CTS	
57	37	29	PTA_7	eADC0_SE3	PTA_7	eTMR0_FLT2	SPI1_PCS3	RTC_CLKIN		UART1_RTS	
58	38		PTA_6	eADC0_SE2	PTA_6	eTMR0_FLT1	SPI1_PCS1			UART1_CTS	
59	39		PTE_7		PTE_7	eTMR0_CH7	eTMR1_FLT0				
60	40	30	VSS	VSS							
61	41	31	VDD	VDD							
62			PTA_17		PTA_17	eTMR0_CH6	eTMR1_FLT0	EWDG_OUT_b			
63			PTB_17		PTB_17	eTMR0_CH5	SPI1_PCS3				
64			PTB_16	eADC0_SE31	PTB_16	eTMR0_CH4	SPI1_SOUT				
65			PTB_15	eADC0_SE30	PTB_15	eTMR0_CH3	SPI1_SIN				
66			PTB_14	eADC0_SE25	PTB_14	eTMR0_CH2	SPI1_SCK				
67	42	32	PTB_13	eADC0_SE24	PTB_13	eTMR0_CH1	eTMR1_FLT1	CAN2_TX	SPI0_PCS2		
68	43		PTB_12	eADC0_SE23	PTB_12	eTMR0_CH0	eTMR1_FLT2	CAN2_RX	SPI0_PCS3		
69	44		PTD_4	eADC0_SE22	PTD_4	eTMR0_FLT3	eTMR1_FLT3				
70	45	33	PTD_3	eADC0_SE19	PTD_3	MPWM0_CH13	SPI1_PCS0	I2C1_SCL	UART1_TX	TMU_IN4	CM33_NMI_b
71	46	34	PTD_2	eADC0_SE18	PTD_2	MPWM0_CH12	SPI1_SOUT	I2C1_SDA	UART1_RX	TMU_IN5	
72	47	35	PTA_3	eADC0_SE17	PTA_3	MPWM0_CH9	I2C0_SCL	EWDG_IN	SPI2_SCK	UART0_TX	
73	48	36	PTA_2	eADC0_SE16	PTA_2	MPWM0_CH8	I2C0_SDA	EWDG_OUT_b	SPI2_SIN	UART0_RX	
74			PTB_11		PTB_11	MPWM0_CH11					
75			PTB_10		PTB_10	MPWM0_CH10					
76			PTB_9		PTB_9	MPWM0_CH9					
77			PTB_8		PTB_8	MPWM0_CH8					
78	49	37	PTA_1	eADC0_SE1/ACMP0_IN1	PTA_1	eTMR1_CH1	SPI2_SOUT		eTMR1_QD_PHA	UART0_RTS	TMU_OUT0
79	50	38	PTA_0	eADC0_SE0/ACMP0_IN0	PTA_0	MPWM0_CH1	SPI2_PCS0		eTMR0_QD_PHA	UART0_CTS	TMU_OUT3
80	51	39	PTC_7	eADC0_SE21	PTC_7	UART1_TX	CAN1_TX	MPWM0_CH11	SPI2_PCS2	eTMR1_QD_PHA	
81	52	40	PTC_6	eADC0_SE20	PTC_6	UART1_RX	CAN1_RX	MPWM0_CH10	SPI2_PCS3	eTMR1_QD_PHB	
82			PTA_16	eADC0_SE29	PTA_16	eTMR1_CH3	SPI1_PCS2				
83			PTA_15	eADC0_SE28	PTA_15	eTMR1_CH2	SPI0_PCS3	SPI2_PCS3			
84	53		PTE_6	eADC0_SE27	PTE_6	SPI0_PCS2		MPWM0_CH15		UART1_RTS	
85	54		PTE_2	eADC0_SE26	PTE_2	SPI0_SOUT	lpTMR0_ALT3	MPWM0_CH14		UART1_CTS	
86			VSS	VSS							

Table 33 continued from previous page

100LQFP	64LQFP	48LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
87			VDD	VDD							
88			PTA_14		PTA_14	eTMR0_FLT0	eTMR1_FLT1	EWDG_IN		eTMR1_FLT0	
89	55	41	PTA_13		PTA_13	eTMR1_CH7	CAN1_TX	SPi0_PCS0	UART2_RX	eTMR0_QD_PHA	
90	56	42	PTA_12		PTA_12	eTMR1_CH6	CAN1_RX	SPi0_SCK	UART2_RX	eTMR0_QD_PHB	
91	57	43	PTA_11		PTA_11	eTMR1_CH5		SPi0_SIN	ACMP0_ACTIVE	I2C1_SCL	
92	58	44	PTA_10		PTA_10	eTMR1_CH4		SPi0_SOUT	RTC_CLKIN	I2C1_SDA	JTAG_TDO_SWD_SWO
93	59		PTE_1		PTE_1	SPi0_SIN		I2C1_SCL	SPi1_PCS0	eTMR1_FLT1	
94	60		PTE_0		PTE_0	SPi0_SCK	TCLK_IN1	I2C1_SDA	SPi1_SOUT	eTMR1_FLT2	
95	61	45	PTC_5		PTC_5	MPWM0_CH0	RTC_CLKOUT	SPi0_PCS1		eTMR0_QD_PHB	JTAG_TDI
96	62	46	PTC_4	ACMP0_IN2	PTC_4	eTMR1_CH0	RTC_CLKOUT		EWDG_IN	eTMR1_QD_PHB	JTAG_TCK_SWD_CLK
97	63	47	PTA_5		PTA_5		TCLK_IN1			eTMR1_QD_PHB	RCU_RESET_b
98	64	48	PTA_4		PTA_4			ACMP0_OUT	EWDG_OUT_b		JTAG_TMS_SWD_IO
99			PTA_9		PTA_9	UART2_TX	SPi2_PCS0			eTMR1_FLT2	eTMR1_FLT3
100			PTA_8		PTA_8	UART2_RX	SPi2_SOUT			eTMR1_FLT3	

7.2 Packages

The information of package pinouts is as follows:

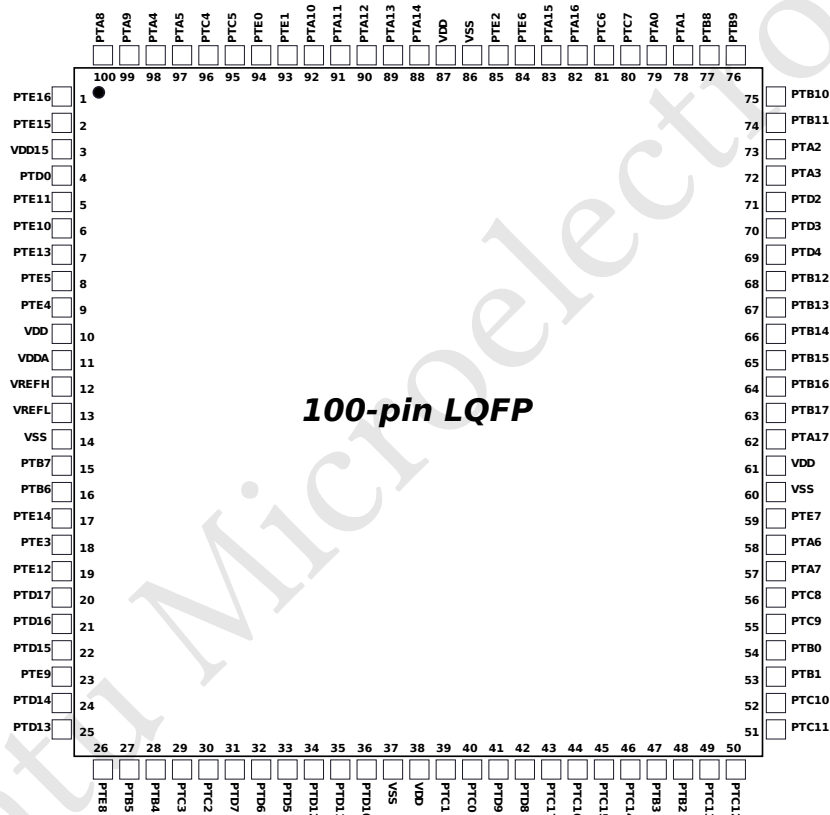


Figure 17: 100-pin LQFP Package

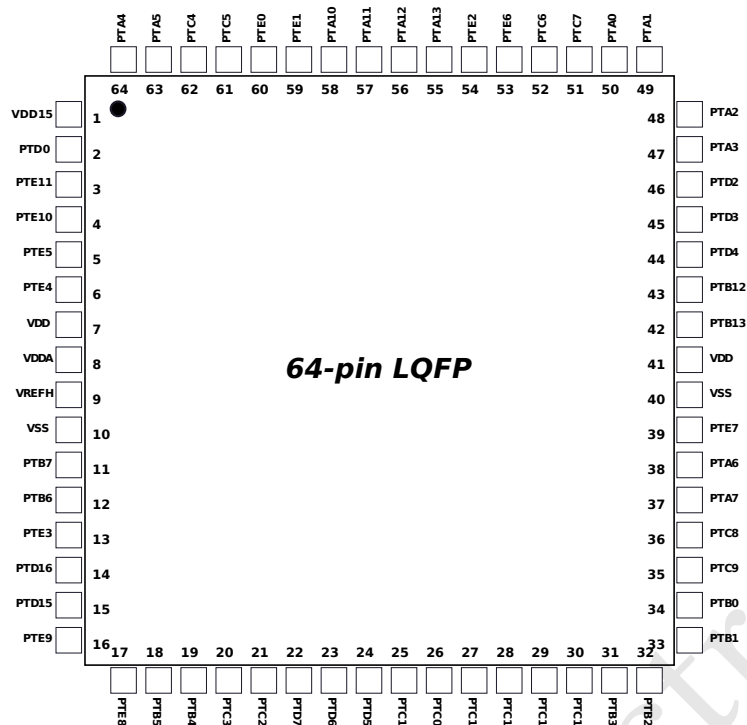


Figure 18: 64-pin LQFP Package

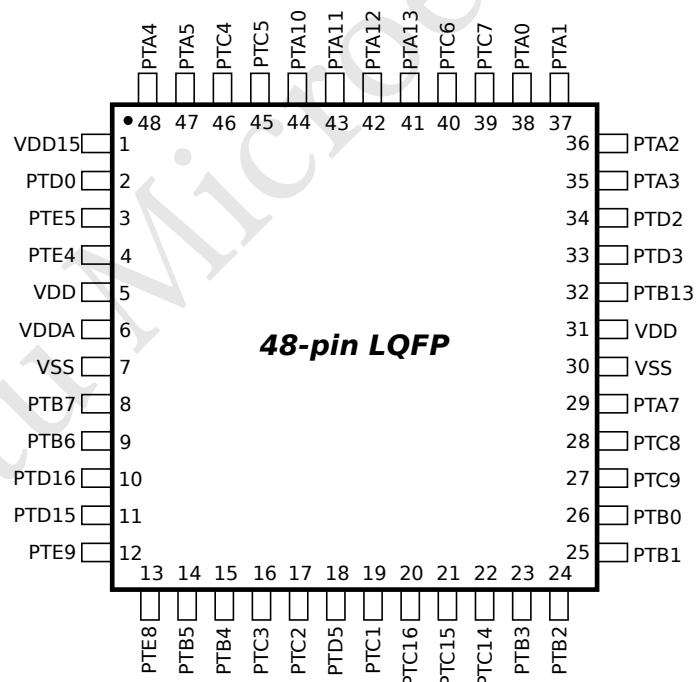


Figure 19: 48-pin LQFP Package

Note: The chip mark will not contain packing information(T/R)

7.3 Dimensions

Package dimensions are as follows:

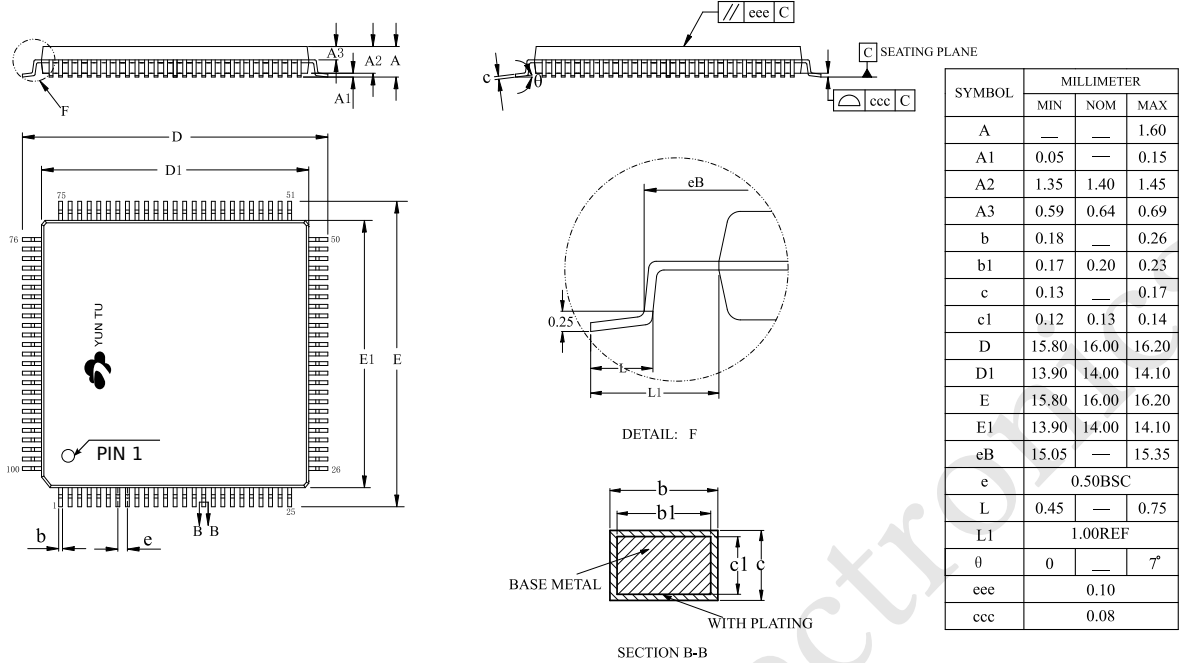


Figure 20: 100pin LQFP

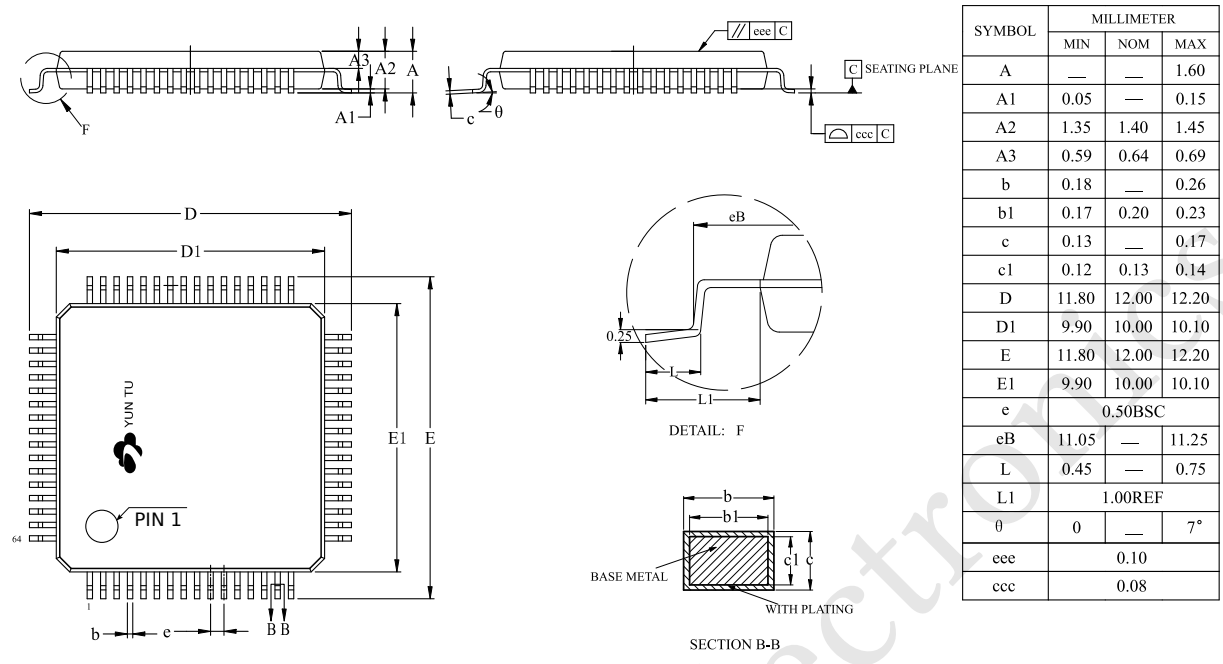


Figure 21: 64pin LQFP

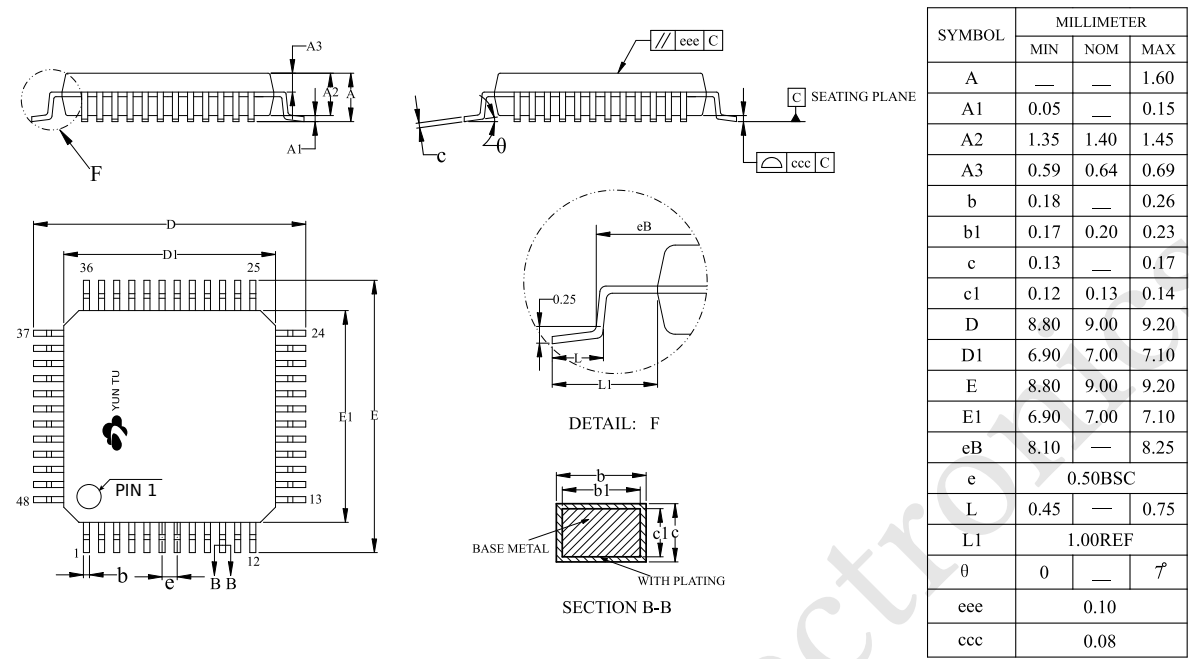


Figure 22: 48pin LQFP

7.4 Reflow Profile Guideline

Reflow Condition:

- can guarantee 3X IR reflow base on the Reflow profile(Figure 5-1) guideline in IPC/JEDEC J-STD-020E;
- Preheat/Soak: Pb-Free Assembly for 150°C~200°C for 60~120s;
- Average ramp-up rate(Ts to peak):3°C/second max.;
- Liquidous temperature maintained above Pb-Free 217°C for 60-150s;
- Time (tp)* within 5°C of the specified classification temperature Pb-Free 30s ;
- Note :

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in this table. For example, if Tc is 260°C and time Tp is 30 seconds, this means the following for the supplier and the user:

For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Table 4-2 Pb-Free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Table 5-2 Classification Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min (T _{smin})	100 °C	150 °C
Temperature Max (T _{smax})	150 °C	200 °C
Time (t _s) from (T _{smin} to T _{smax})	60-120 seconds	60-120 seconds
Ramp-up rate (T _L to T _p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T _L)	183 °C	217 °C
Time (t _L) maintained above T _L	60-150 seconds	60-150 seconds
Peak package body temperature (T _p)	For users T _p must not exceed the Classification temp in Table 4-1. For suppliers T _p must equal or exceed the Classification temp in Table 4-1.	For users T _p must not exceed the Classification temp in Table 4-2. For suppliers T _p must equal or exceed the Classification temp in Table 4-2.
Time (t _p)* within 5 °C of the specified classification temperature (T _c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T _p to T _L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

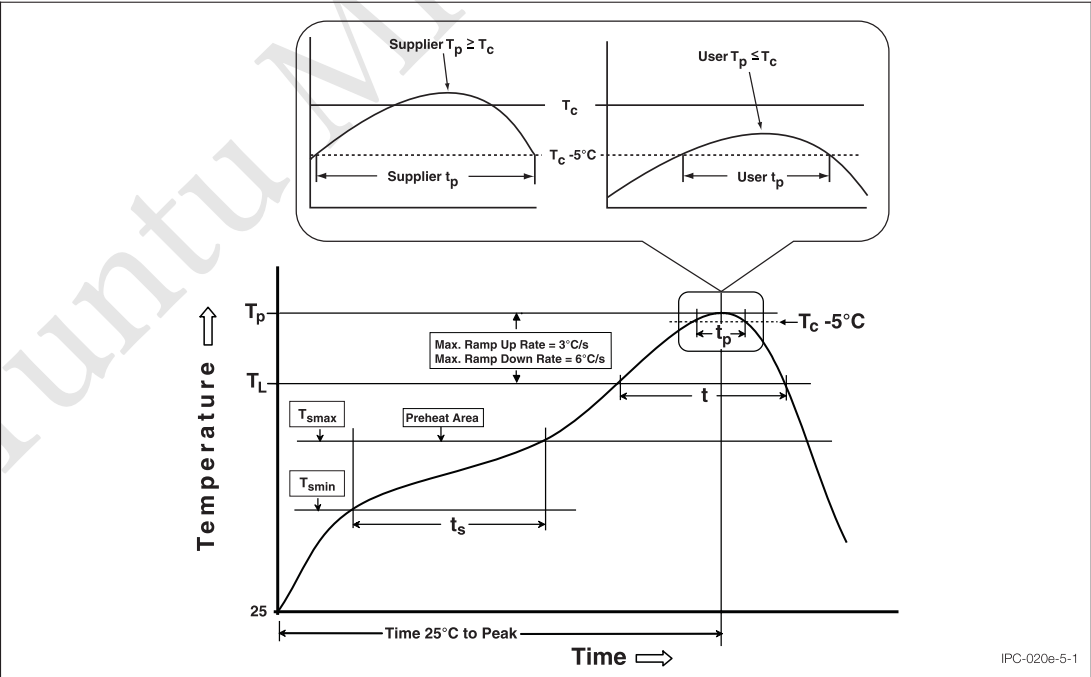


Figure 5-1 Classification Profile (Not to scale)

Figure 23: Reflow Profile Guideline

Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2025/8/13	Initial version
1.1	2026/2/25	Corrected ADC internal channel to 4 in chapter of “Features Summary” Corrected the FlexCAN number to 3 in table of “Ordering information” Added the chip storage conditions in subsection of “Moisture Handling Ratings” Corrected the value of I_{oh} and I_{ol} in subsection of “DC Electrical Specifications at 3.3V” Added the value of V_{bg} , V_{DD15} and note in subsubsection of “LVR and LVD Operating Requirements” Updated the Min and Max value in subsection of “Power Consumption” Added the whole subsubsection of “MCU Power Supply Ramp Rate” Updated Min value of V_{PP} and information of gm in subsection of “FXOSC(4-40MHz) Characteristics” Added the clock source information in subsection of “FIRC(48MHz) Characteristics” Added the clock source information in subsection of “SIRC(2MHz) Characteristics” Corrected typical value of C_p in subsection of “ADC Characteristics” Added the section of Reflow Profile Guideline in chapter of “Pinouts”

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