YTM32B1HA0x Data Sheet

Support: YTM32B1HA01G0MLUT, YTM32B1HA01G0MLQT, YTM32B1HA01G0MLLT

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1 Features Summary

- AEC-Q100 qualified
- ASIL-D compliant
- Arm Cortex-M7 with lockstep, up to 200 MHz
- Memories
  - 8 KB I-Cache, 8 KB D-Cache with ECC support
  - Up to 2 MB Program Flash memory and 256 KB Data Flash with ECC support, and support OTA
  - Up to 256 KB OCRAM, supports ECC feature, and includes 32 KB OCRAM block which supports data retention in Powerdown mode
  - Up to 32 KB ITCM and 128 KB DTCM with ECC support
  - 32 bytes register file (REGFILE) which supports data retention in Powerdown mode
  - 64 KB ROM with ECC support
- Provide multiple clock sources including:
  - 96 MHz Fast Internal RC Oscillator (FIRC)
  - 4~40 MHz Fast Crystal Oscillator (FXOSC)
  - Up to 200 MHz Phase-Locked Loop (PLL)
  - 12 MHz Slow Internal RC Oscillator (SIRC)
  - 32.768 KHz Slow Crystal Oscillator (SXOSC)
- Power Control Unit (PCU) with internal regulators capable of supporting multiple power modes
  - Active
  - Sleep
  - Deepsleep
  - Standby
  - Powerdown
- Support up to 64 WKU pins to wake up from Powerdown mode
- 32 DMA channels with up to 111 hardware trigger sources
- I/O supporting 2.97 ~ 5.5 V supply
- Wide operating voltage ranges (2.97 ~ 5.5 V) with fully functional flash memory program/erase/read operations
- Debug functionality
  - Joint Test Action Group (IEEE 1149.1 standard)
  - Serial Wire Debug (SWD)
- Human-machine interface
  - Up to 154 general-purpose input/output (GPIO)
  - External interrupt
- Analog
  - Two 12-bit, 2Msps SAR ADCs, up to 2x32 external channels and 8 internal channels
  - Two On-chip Analog Comparators (ACMPs) with 8-bit DAC, up to 2x8 channels
  - Support temperature sensor
- Timers
  - Two Timer (TMR) modules
  - Three Periodic Timer (pTMR) modules with 4 channels respectively
  - One Low Power Timer (lpTMR)
  - Six Enhanced Timer (eTMR) modules with 8 channels respectively
  - Three Multiple Pulse Width Modulation (MPWM) modules with 16 channels respectively
  - One Real-Time Clock (RTC)
  - Two Programmable Trigger Unit (PTU) modules
- Serial communication interfaces
  - Eight FlexCAN modules with FD
  - Ten LINFlexD modules
  - Eight Serial Peripheral Interface (SPI) modules
  - One Quad Serial Peripheral Interface (QSPI) module
  - Five Inter-Integrated Circuit (I2C) modules
  - Two Single Edge Nibble Transmission (SENT) modules with 4 channels respectively
  - One ENET module with TSN
  - Two Serial Audio Interface (SAI) modules
- Security, integrity and safety
  - Programmable Cyclic Redundancy Checker (PCRC)
  - Hardware Cryptography Unit (HCU) which supports AES/SM4/SHA
  - True Random Number Generator (TRNG)
  - Clock Monitor Unit (CMU)
  - Watchdog (WDG)
  - MPU for dynamic task protection (16 regions)
  - Peripheral Protection Unit (PPU)
  - Interrupt Monitor (INTM)
  - ECC Management Unit (EMU)
  - Fault Management Unit (FMU)
- Temperature range
  - Ambient operating temperature: -40 °C ~ 125 °C
  - Junction operating temperature: -40 °C ~ 150 °C
- Package options
  - 176-pin LQFP
  - 144-pin LQFP
  - 100-pin LQFP

Contents

2 Overview

YTM32B1HA0x series provide the highly scalable portfolio of ARM® Cortex®-M7 MCUs in the automotive industry. With 2.97 ~ 5.5 V supply and focus on exceptional EMC/ESD robustness, YTM32B1HA0x series devices are well suited to a wide range of applications in electrical harsh environments, and are optimized for cost-sensitive applications offering low pin-count option.

The YTM32B1HA0x series offer a broad range of memory, peripherals and package options. They share common peripherals and pin counts allowing developers to migrate easily within an MCU family or among the MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the YTM32B1HA0x series for their end product platforms, maximizing hardware and software reuse and reducing time-to-market.

3 Block Diagram

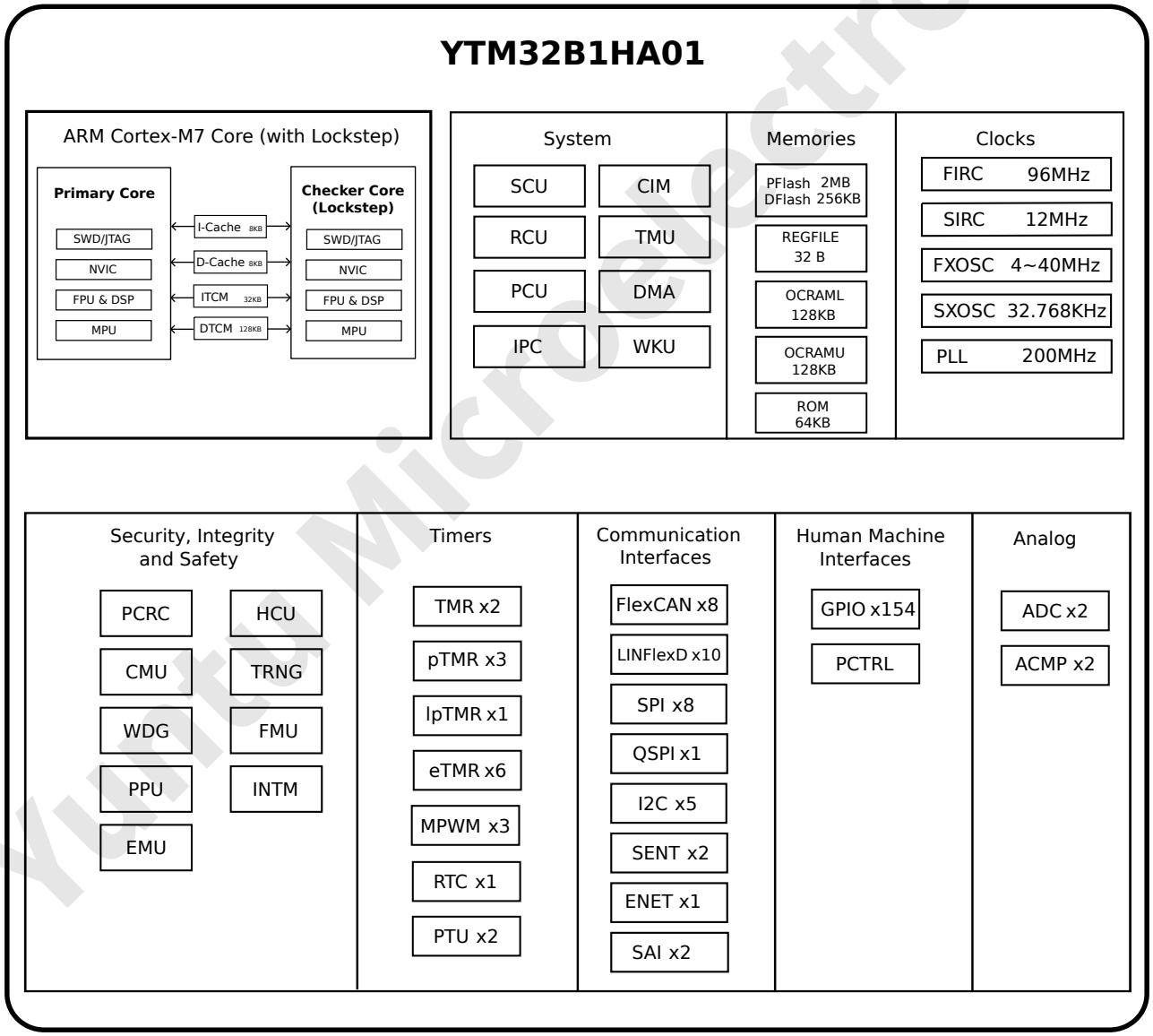


Figure 1: YTM32B1HA01 Block Diagram

4 Features

4.1 Core Modules

4.1.1 ARM Cortex-M7

- An in-order issue, super-scalar pipeline with dynamic branch prediction
- DSP extensions
- The ARMv7-M Thumb instruction set, defined in the Arm v7-M Architecture Reference Manual
- Banked Stack Pointer (SP)
- Hardware integer divide instructions, SDIV and UDIV
- Handler and Thread modes
- Automatic processor state saving and restoration for low-latency Interrupt Service Routine (ISR) entry and exit
- Support for ARMv7-M unaligned accesses
- Low-latency interrupt processing
- A low-cost debug solution with CoreSight components
  - Support breakpoints
  - Support watchpoints, tracing, and system profiling
  - Support printf() style debugging through an Instrumentation Trace Macrocell (ITM)
  - Support Trace Port Interface Unit (TPIU)
  - Support Debug Access Port (DAP)
- Support ETM (Embedded Trace Macrocell)
- Support Floating Point Unit(FPU)
- Support WIC
- Support memory interfaces that include
  - Harvard architecture-based instruction and data caches, and an AXIM interface
  - A dedicated low-latency AHBP interface
  - A 64-bit AXI AMBA4 memory interface with a 8 KB instruction cache and an 8 KB data cache for efficient access to external resources. The instruction and data caches are ECC protected.
  - A 32-bit AHBS for interfacing with slaves
  - 64-bit and 32-bit memory interfaces for the connection to local Tightly Coupled Memories called ITCM and DTCM
  - Cortex-M7 core interfaces with low-latency 32 KB ITCM, 64 KB DTCM0 and 64KB DTCM1
  - Support 16 regions MPU

4.1.2 Vector Fetch Behavior on Cortex-M7

In Cortex-M7, the vector fetches are looked up into the I-Cache. If the vector table is located in a region of memory that is cacheable, any load or store to the vector must be treated as self-modifying code and cache maintenance instructions should be used to synchronize the updates to the data and instruction caches.

The Cortex-M7 Device Generic User Guide chapter ‘Cache maintenance design hints and tips’ specifies a recommendation for synchronization of the D-Cache and I-Cache.

If cache maintenance is to be avoided each time when the vector table gets updated, then the vector table must be allocated in the ITCM or DTCM, as those are non-cacheable regions. Alternatively, the I-Cache must be enabled after the vector table has been initialized.

4.1.3 Debug Controller

- Extensive debug capabilities such as run control and tracing
- Includes the standard Arm debug port that supports the JTAG and SWD interfaces
- Debug can be disabled by programming flash CUS_NVR with special words

4.2 System Modules

4.2.1 System Clock Unit (SCU)

- Fast Internal RC Oscillator(FIRC)
  - Up to 96 MHz
  - Default system boot clock source
  - Supports trim for temperature and process
  - Can be selected as PLL reference clock
- Slow Internal RC Oscillator(SIRC)
  - Up to 12 MHz
  - Can be selected as system clock source
  - Always on unless it is forced to be disable in Deepsleep, Standby and Powerdown mode
  - Supports trim for temperature and process
- Fast Crystal Oscillator(FXOSC)
  - Supports 4~40MHz crystal
  - Can be selected as PLL reference clock
  - Can be selected as system clock source
  - Supports bypass mode
- Slow Crystal Oscillator(SXOSC)
  - 32.768 KHz real time oscillator
  - Can’t be selected as system clock
  - Provides accurate clock as the functional clock sources of some peripherals and Real-Time Clock(RTC)
- Phase-Locked Loop(PLL)
  - Up to 200 MHz
  - Contains Voltage-Controlled Oscillator(VCO)
  - Supports selectable reference clock
  - Contains frequency lock detector
  - Can be selected as system clock source
- Clock Monitor Unit (CMU)
  - SCU contains 4 CMU blocks
  - CMU monitors slow bus clock, FIRC clock, PLL clock and FXOSC clock
  - FXOSC or SIRC clock can be selected as reference clock of CMU
  - CMU can detect frequency out of range, loss of checked clock and loss of reference clock
- SCU provides glitch free switcher to select system clock source
- SCU provides system clock dividers to generate core clock, fast bus clock and slow bus clock

4.2.2 Power Control Unit (PCU)

- Combination of internal and external voltage regulator options, offering a variety of power modes
- Active POR providing brown-out detect
- Low Voltage Reset (LVR) for all system relevant power domains
- High Voltage Detect (HVD) as indication for software.

4.2.3 Reset Controller Unit (RCU)

- Record the reset sources of most recent resets
- Configurable filter for reset pin
- Reset pin filter can work at both active and low power mode

4.2.4 IP Controller (IPC)

- Peripheral Bus clock enable
- IPC clock source selection as follow
  - FIRC 96MHz
  - SIRC_DIV4_CLK 3MHz
  - FXOSC 4~40MHz
  - SXOSC 32.768KHz
  - PLL 200MHz
  - FAST_BUS_CLK
- IPC clock divide values from 1 to 16
- Peripheral software reset

4.2.5 Wakeup Unit (WKU)

- Support for up to 64 external input pins and up to 4 internal modules with individual enable bits for MCU interrupt from Powerdown mode
- Input sources may be external pins or from internal modules capable of running in Powerdown mode
- External input pins programmable for falling-edge, rising-edge, or any-edge detection
- Support to enable external input pin and filter detection in Powerdown mode
- Optional digital filters provided to qualify an external pin detect. Note that when the SIRC and SXOSC clock is disabled, filters are disabled and bypassed

4.2.6 Direct Memory Access (DMA)

- All address range data transfer from source to destination
- Support separate source/destination data size configuration
  - Double word(64-bit), word(32-bit), half word(16-bit), byte(8-bit) transfer size
- Support separate source/destination address offset configuration
  - Address increase/decrease/keep selectable
- Up to 32 DMA channels
  - Fix priority and round-robin arbitration
  - Support channel to channel link
- Software/Hardware/Link trigger
- Up to 128 peripheral hardware triggers
- Internal data fifo for data transfer
- Support update DMA transfer information from system memory after transfer complete
- Support data transfer loop and trigger loop

4.2.7 Trigger Multiplex Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources

4.2.8 Chip Integration Module (CIM)

- System clocking configuration
- ADC and ACMP trigger selection
- Software trigger generate
- Software fault generate
- eTMR external clock, fault and channel input selection
- eTMR output modulation configuration
- ENET clocking configuration
- FPU interrupt enable
- TCM backdoor access enable
- System boot configuration
- System unique identification (UID) device
- Flash memory and system RAM size configuration
- Package configuration
- FlexCAN FD feature configuration

4.3 Memories

4.3.1 Embedded Flash Module (EFM)

- Two Program-Flash (PFlash0 and PFlash1) with ECC
  - Each PFlash includes 1 MB main array
  - Each PFlash block includes 512 sectors, and valid data size of each sector is 2KB
  - 16KB OTP (One-Time Programmable)
  - 4KB AES key storage
  - Support Read-While-Write (RWW) and Over-The-Air (OTA) technology
- One Data-Flash (DFlash) with ECC
  - 256 KB main array
  - Include 256 sectors, and valid data size of each sector is 1KB
- Protection scheme against accidental program or erase operations
- Command protection function for authorization protection
- Optional interruptions on command completion and status update

4.3.2 Register File (REGFILE)

- 32 bytes register file to retain value during Powerdown mode
- Access through APB bus

4.3.3 On-Chip RAM (OCRAM)

- Up to 256KB
- Support 64/32/16/8bit access
- Support ECC safety function
  - 64bit data and 8bit ECC code
  - Single bit error correction
  - Double bit error detection
- Support RAM retention in power down mode(32KB RAM which mapped to 0x2002_0000~0x2002_7FFF)

4.3.4 Tightly Coupled Memory (TCM)

- 32KB ITCM and 128KB DTCM
- Support ECC function
- Support backdoor access by other AHB masters

4.3.5 Read-Only Memory (ROM)

- 64KB on-chip memory map
- The ROM boot firmware is programmed by YTMicro to support the following four functions: Secure boot, Fast wakeup from Powerdown Mode, Structural Core Self-Test (SCST), System clock and watchdog configuration:
  - Run once the chip releases the reset signal of the CM7 core
  - Support the parsing of the configurable BVT (Boot Vector Table) stored in the Flash memory
- Secure boot
  - Work as the root of trust
  - Support CMAC authorization of the customized code (i.e. bootloader, OTA) with the specified secure boot group configuration set in the BVT.(Note: The CMAC authorization is achieved by HCU.)
    - Support decryption of secure boot section configuration structure with the specified HCU AES key in secure boot group configuration
    - Support up to 8 secure boot section configurations (each includes the section start address, length and HCU AES key used for CMAC as well as CMAC stores address pointer)
  - The used HCU hardware user keys for secure boot section configuration structure encryption and CMAC authorization should be pre-programmed to HCU_NVR memory by the Car OEM or Tier-1 using the flash programmer
  - Support strict serial secure boot mode (enabled via BVT)
    - If CMAC authorization fails, the secure boot holds the CM7 core in static mode
  - Support normal serial secure boot mode (by default)
    - If CMAC authorization fails, the CM7 core continues to execute the bootloader and the applications, but all HCU hardware user keys will be disabled or fail to load.
- Fast wakeup from Powerdown Mode
  - Support fast wakeup when recovering from Powerdown mode
  - Reduce the ROM boot time by waiving the execution of secure boot and core test
  - Support for the enabling and configuration of the separated IVT (Interrupt Vector Table), by using the first two words of REGFILE that are retained during the Powerdown mode
- Structural Core Self-Test (SCST)
  - YTMicro provides the code for the CM7 core test, for the purpose of latent fault detection, which is an important safety mechanism of the CM7 core to aid the FuSa ASIL-D
- System watchdog configuration
  - Support watchdog enable/disable function and timeout configuration for CM7 main core (The default clock source of WDG in IPC will be selected to SIRC/4)

4.4 Analog

4.4.1 Analog-to-Digital Converter (ADC)

- Contain two ADC instances
  - ADC0 supports up to 32 external analog input channels, and 8 internal channels
  - ADC1 supports up to 32 external analog input channels
- Support 12-bit, 10-bit, 8-bit, and 6-bit single-ended configurable resolution
- Up to 2Msps for 12-bit resolution conversion performance

- Support DMA and conversion result FIFO with watermark
- Support multiple conversion modes
  - Single mode
  - Continuous mode
  - Discontinuous mode
- Support software/hardware trigger for ADC start conversion
- Support two power saving modes
  - Wait mode: prevent ADC overrun when FIFO is full
  - Auto off mode: automatic control ADC power off
- Support watchdog for conversion result monitoring
- Support automatic calibration
- Support interrupt generate
  - Ready for conversion
  - End of sampling
  - End of conversion
  - End of sequence conversion
  - Overrun event
  - Watchdog event
- Support work and wake up when the chip under low power mode
- Support self-test mode

4.4.2 Analog Comparator (ACMP)

- Contain two ACMP instances
- Each ACMP supports 8 channels
- Operational over the entire supply range
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable inversion on comparator output
- Function mode
  - Common mode
  - Sample mode
  - Window mode
  - Continuous mode
    - One-Shot mode
    - Loop mode
- All channels can be used to execute automatic comparison
- Support digital filter, the filter can be bypassed
- Two software selectable performance levels
  - Shorter propagation delay at the expense of higher power
  - Low power with longer propagation delay
- Functional in all power modes
- Support independent 8-bit DAC output to the comparator
- Support DAC output to pin
- Support several interrupts
  - For common/sample/window mode
  - Generate interrupt on rising-edge, falling-edge or both edges of the comparator output
  - For continuous mode
  - Generate interrupt when the comparison results don’t match with expectations
- Interrupt can be generated without any clock in common mode

- A comparison event can be selected to trigger DMA transfer

4.5 Timers

4.5.1 Timer (TMR)

- One 32-bit count-up timer with an 8-bit prescaler
- Four 32-bit compare channels
- An independent interrupt source for each channel
- Ability to stop the timer in debug mode

4.5.2 Periodic Timer (pTMR)

- Four channels of 32bit timers, each timer has independent timeout periods
- Timers can generate interrupts, and each channel can generate independent interrupt request
- Support chain mode to connect multiple timer to a longer timer
- Ability to stop in debug mode

4.5.3 Low Power Timer (lpTMR)

- 16-bit time counter or pulse counter with compare
- Optional interrupt can generate asynchronous wakeup from any low-power mode
- Hardware trigger output
- Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

4.5.4 Enhanced Timer (eTMR)

This chip contains 6 eTMRs (eTMR0, eTMR1, eTMR2, eTMR3, eTMR4, eTMR5), their features are divided into common features and individual features.

The common features of all eTMRs are listed below:

- Configurable initial and final counter values
- Contain 8 channels
- Support two clock sources
  - Bus clock
  - External clock
- Support 7-bits clock prescaler
- Support four channel modes
  - Common timer
  - PWM mode
    - Independent mode for each channel
    - Complementary mode for each pair of channels
      - All channels support independent deadtime insertion
    - Support dithering
    - Channel output control (initialization, software control, mask control, double switch control, fault control)
      - Support 4 fault input sources

        - Support fault input from TMU or pad
        - Support fault input polarity control
        - Support fault input filter
        - Support fault input stretch
        - Support fault event generated by combinational logic
      - Relevant registers have buffer registers and support loading mechanism
    - Output Compare mode
      - The output can be configured to set, clear or toggle on match point
    - Input Capture mode
      - Support rising edges, falling edges or dual edges capture
      - Support input filter with a prescaler
      - Support capture test mode
      - Support pulse width measure
- Support generating triggers
  - Output triggers with adjustable pulse width on match point
  - Output pulse with adjustable width by PWM
- Polarity control is available for each channel
- Support GTB (Global Time Base)
- Support several interrupts
  - Channel interrupt (capture interrupt and compare interrupt)
  - Counter overflow interrupt
  - Fault event interrupt
- Support DMA
- Support counter running under debug mode
- Support input from ACMP
- Support hall sensor input

The individual features are listed below:

- Counter
  - eTMR3 has a 32-bit counter
  - Other eTMRs have a 16-bit counter
- eTMR1 and eTMR2 support quadrature decoder mode
  - Contain a independent 16-bit counter with a clock prescaler
  - Support 4 up-down counting modes
  - Support phase A and phase B input filter
  - Support quadrature decoder counter overflow interrupt
- eTMR0 and eTMR3 support modulated output

4.5.5 Multiple Pulse Width Modulation (MPWM)

This chip contains 3 MPWMs(MPWM0, MPWM1, MPWM2). The features are listed below:

- Each MPWMx supports 16 channels
- Each channel contains a 16-bit counter independently
  - Configurable comparison value
  - Configurable period value
- Support clock prescaler(1, 2, 4, 8, 16, 32, 64, 128) independently
- Counting modes
  - Continuous mode
  - One shot mode

- Support counter starts counting by hardware trigger in one shot mode
- Support four channel modes
  - Common timer
  - PWM mode
    - Independent mode for each channel
    - Support edge-aligned PWM
    - Relevant registers have double buffer registers and Support loading mechanism
    - Write operations to double buffer registers take effect immediately
  - Output Compare mode
    - The output can be configured to set, clear or toggle on match point
  - Input Capture mode
    - Support rising edge capture
    - Support falling edge capture
    - Support any edge capture
  - Pulse count mode
- Support generating triggers on match point
- Polarity control is available for each channel
- Support several interrupts
  - Channel event interrupt
  - Timer overflow event interrupt
- Support DMA
- Support counter running under debug mode

4.5.6 Real-Time Clock (RTC)

- Register write protection for RTC enable register
- 32-bit seconds counter with overflow flag and optional interrupt
- Configurable 32-bit alarm
- Configurable 1, 2, 4, 8, 16, 32, 64 or 128 Hz square wave output with optional interrupt

4.5.7 Programmable Trigger Unit (PTU)

- Contain two PTU instances
- 8 configurable PTU channels for ADC hardware trigger
- Each trigger outputs can be enabled/disabled independently
- Configurable delay per pre-trigger output
- Support bypass of pre-trigger delay
- Support software trigger source
- Support continuous mode
- Support interrupt delay
- Support pulse output as ACMP’s sample window

4.6 Security, Integrity and Safety

4.6.1 Programmable Cyclic Redundancy Check (PCRC)

- Programmable CRC polynomials
- Programmable initial seed
- Optional bit-swap in one byte is available for input and output data
- Optional bit-swap in one word is available for input and output data

- Optional byte-swap in one word is available for input and output data
- Optional bit-inversion is available for output data
- 8/16/32-bit access for CRC input data

4.6.2 Hardware Cryptography Unit (HCU)

- Support 128-, 192- and 256-bit key length
- Support both encryption and decryption
- Support secure hardware key and flexible software key
- Support several algorithm engines
  - AES (ECB, CBC, CTR, CCM, CMAC)
  - SM4 (ECB)
  - SHA (SHA-256, SHA-384)
- All data input/output are in little-endian format
- Support bit, byte and half-word data swapping
- Size of input/output FIFO is up to 32*32 bits
- Support DMA transport between chip memory and input/output FIFO
- Support several interrupts
  - Operation done interrupt
  - Input FIFO empty interrupt
  - Output FIFO full interrupt
  - Input FIFO overflow interrupt
  - Output FIFO underflow interrupt
  - Input/output FIFO watermark interrupt
- Clock gating strategy is applied for engine core when input/output FIFO is not ready

4.6.3 True Random Number Generator (TRNG)

- Generate a 256-bit entropy
- Monobit test to limit the number of value 0 and 1
- Long run test to avoid continuous constant value
- 1 ring OSC with clock checker
- 3 interrupt sources
  - Entropy valid interrupt
  - Frequency error interrupt
  - Hardware error interrupt

4.6.4 Watchdog (WDG)

- 32-bit countdown timer
- Functional clock can be selected from IPC and bus clock
- Support regular or window servicing mode
- Support reset request or interrupt for the first timeout
- Hard and soft configuration lock bits

4.6.5 Peripheral Protection Unit (PPU)

- Write access for the module under protection can be restricted to the supervisor mode only
- Maximum 4KB register slot size of module under protection
- Multiple ways are present to set the lock bits

- Once the lock bits are set, the registers could be protected from modification

4.6.6 Interrupt Monitor (INTM)

- Up to 4 programmable monitors
- Programmable monitored interrupt source per monitor
- Programmable 24-bit counter threshold per monitor
- Timer expired status bit per monitor
- One overall interrupt acknowledge for all monitors
- One overall enable for all monitors

4.6.7 ECC Management Unit (EMU)

- Multiple channels of ECC injection and report
- Two-stage enable mechanism for ECC injection
- Location and correctable or uncorrectable error can be injected
- ECC error interrupt can be enabled with separated register bit
- The last ECC error data can be recorded into register

4.6.8 Fault Management Unit (FMU)

- Support up to 36 fault channels from safety relevant functions on the device
- Configurable FMU clock sources
  - SIRC_DIV4
  - FIRC
  - SXOSC
  - FXOSC
  - PLL
- Software fault recovery management
- Fault injection
- Lockable fault configuration
  - Changes are possible in CFG state only
  - Configuration changes observed by CFG counter
- Configurable fault control
- Support up to 4 fault inputs via IO (FMU_ERR_IN function)
- Support 2 outputs for fault indication via IO (FMU_ERR_OUT function)
  - Configurable output window
  - Configurable output polarity
- Configurable chip reactions for each fault
  - Alarm interruption (for ALARM state)
  - FMU functional reset
  - NMI
  - No reaction
- Configurable chip reactions for fault input(FMU_ERR_IN)
  - FMU functional reset
  - NMI
- Support FMU Fail To React (FFTR) detection
  - Configurable FFTR counter timeout threshold
  - Support FFTR event reset chip

4.7 Communication Interfaces

4.7.1 Flexible Controller Area Network (FlexCAN)

- Full implementation of the CAN FD protocol and CAN Specification 2.0, Part B
  - Standard data frames
  - Extended data frames
  - Zero to sixty-four bytes data length
  - Programmable bit rate
  - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Silicon-proven implementation passing ISO 16845-1:2016 CAN conformance tests
- Flexible mailboxes configurable to store 0 to 8, 16, 32, or 64 bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Legacy Rx FIFO with storage capacity for up to 6 CAN frames and automatic internal pointer handling with DMA support
- Full-featured Enhanced Rx FIFO with storage capacity for up to 32 CAN FD frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Flexible message buffers, totaling 128 message buffers of 8 bytes data length each, configurable as Rx or Tx
- Programmable clock source to the CAN Protocol Engine, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer, with an optional external time tick or high-resolution 32-bit on-chip timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low-Power modes, with programmable Wake-Up on bus activity or matching with received frames (Pretended Networking)
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the FlexCAN is synchronous with CAN bus
- CRC status for transmitted message
- Legacy Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Legacy Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 ID Filter Table elements
- Powerful Enhanced Rx FIFO ID filtering, capable of matching incoming IDs against either 64 extended or 128 standard ID filter elements with three filtering schemes: mask + filter, range, and two filters without mask
- 100% backward compatibility with previous FlexCAN version
- Supports detection and correction of errors in memory read accesses. Each byte of FlexCAN memory is

associated to 5 parity bits. The error correction mechanism ensures that in this 13-bit word, errors in one bit can be corrected (correctable errors) and errors in 2 bits can be detected but not corrected (non-correctable errors).
- Supports Pretended Networking functionality in Low-Power modes: Deepsleep mode

4.7.2 Local Interconnect Network (LINFlexD)

- LINFlexD common features in both LIN and UART
  - Fractional baud rate generator
  - Three operating modes for power saving and configuration registers lock
    - Initialization
    - Normal
    - Sleep
  - Test mode: Loop Back
  - Maskable interrupts
- LIN mode features
  - Support for LIN protocol versions 1.3, 2.0, 2.1, and 2.2
  - Bit rates up to 20 Kbit/s (LIN protocol)
  - Master/slave modes
  - Classic and enhanced checksum calculation and check
  - Single 8-byte buffer or FIFO for transmission/reception
  - Timeout management
  - Identifier filters
  - DMA interface
  - Support for 16 identifiers
  - Master mode with autonomous message handling
  - Wakeup event on dominant bit detection
  - True LIN field state machine
  - Advanced LIN error detection
  - Header, response, and frame timeout
  - Slave mode
    - Autonomous header handling
    - Autonomous transmit/receive data handling
  - Identifier filters for autonomous message handling in slave mode
  - Separate clock for baud rate calculation
- UART mode features
  - Full-duplex communication
  - Separate clock for baud rate calculation
  - Baud rate is a function of baud clock, and the LINIBRR and LINFBRR registers.
  - 7/8 bits data, parity
  - 1/2/3 stop bits
  - 12-bit + parity reception
  - 4-byte buffer for reception; 4-byte buffer for transmission
  - 12-bit counter for timeout management
  - The maximum baud rate achievable is baud clock/4 Mbit/s
  - For bit rate ≤ baud clock/16 Mbit/s
    - 16 times oversampling
    - 3:1 majority voting
  - For baud clock/16 Mbit/s < bit rate ≤ baud clock/8 Mbit/s
    - Reduced oversampling programmable by software

    - 3:1 majority voting for reduced oversampling of 8 samples per bit
  - For baud clock/8 Mbit/s < bit rate ≤ baud clock/4 Mbit/s
    - Reduced oversampling programmable by software
    - 1:1 voting for all reduced oversampling of 4, 5, and 6 samples per bit

4.7.3 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration
- Configurable frame size
- Transmit/Receive FIFO
- Support single line mode
- Support Master and Slave mode
- Support Transmit/Receive via DMA

4.7.4 Quad Serial Peripheral Interface (QSPI)

- Flexible programmable sequence engine to support various vendor devices
  - Serial NOR Flash
  - Serial NAND Flash
  - HyperBus device (HyperFlash/HyperRAM)
- Support max to 4 LUT sequences, each LUT sequence contains 10 instructions
- Support single, dual, quad, and octal access modes for serial flash memories
- Support two sets of independent flash interfaces
- Support individual/parallel mode
- Support for XIP (Execute in Place)
- Support for SDR (100MHz) and DDR (50MHz) mode
- Support multi-master accesses
- Support delay chain for input clock sampling data
- 32*32 TxFIFO for data write with DMA support
- 32*32 RxFIFO for data read with DMA support
- 64*32 buffer for AHB access
- Support 128MB AHB access size (0x68000000~0x6FFFFFFF)
- Support serial flash clock stopped when RxFIFO is full

4.7.5 Inter-Integrated Circuit (I2C)

- Support standard, fast and ultra fast mode
- Support 7-bit/10-bit address mode with master and slave
- Support SMBus mode
- Support multi-master arbitration and synchronization
- Support Master and slave clock stretching
- Transmit/Receive FIFO (Master only)
- Analog and digital filter on both SCL and SDA pins
- Support Transmit/Receive via DMA

4.7.6 Single Edge Nibble Transmission (SENT)

This chip contains two SENTs (SENT0 and SENT1), and they have the same features:

- Always acts as a receiver

- Support selectable functional clock for message receiving
- Support four channels for different devices
- Support SENT protocol specification J2716 JAN2010
- Support programmable input filter for each channel
- Support configurable receive tick times from 3μs to 90μs for each channel
- Support auto compensation for variation in SENT transmit clock up to $\pm$ 25%
- Support configurable number of data nibbles for each channel
- Support status nibble optionally included in the checksum
- Support pause pulse for each channel
- Support separate channel buffer for storing Fast and Slow Serial Message
- Support FIFO mode to store Fast Message from all channels (Depth 16)
- Support DMA to access Fast and Slow Serial Message
- Support time stamp for all receive message
- Support varied interrupts
  - Fast Message receive interrupt
  - Slow Serial Message receive interrupt
  - Channel receive error interrupt
  - FIFO/buffer overflow and underflow interrupt
  - Wake up interrupt (any channel busy to trigger)

4.7.7 ETHERNET (ENET)

ENET supports these features in addition to the default feature defined in the IEEE802.3 specification:

- MII (10/100 Mbps), RMII (10/100 Mbps)
- Time-aware shaper (IEEE802.1bv), time synchronization (IEEE802.1AS-rev), and frame preemption (IEEE802.1Qbu) for time-sensitive networking
- Media clock recovery and generation for AVB
- AMBA 2.0 for AHB master and APB3 interface
- RMII specification version 1.2 from RMII consortium
- Separate interface for transmit, receive, and control paths
- Two-buffer ring
- Broadcast and multicast packet duplication
- Full-duplex flow control operations (IEEE 802.3x pause packet and priority flow control)
- Network statistics with MAC management (RMON) counters
- Flexibility to control the pulse per second (PPS) output signal
- MDIO clause 22 and clause 45 interface for configuration and management of the PHY device
- Preamble and SFD insertion and deletion
- Automatic CRC and pad generation/stripping option
- Option to disable CRC checking
- Programmable insert packet gap
- Source address insertion or replacement
- VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control, insertion, replacement, and deletion of up to two VLAN tags, insertion, replacement, and deletion of queue or channel-based VLAN tags
- IEEE802.1Q VLAN tag detection and an option to delete the tags in the receive packets
- Programmable safety watchdog timeout limits
- Flexible address filtering modes that allow
  - Up to two additional 48-bit perfect DA filters with masks for each byte

  - Up to two 48-bit SA comparison checks with masks for each byte
  - 64-bit hash filter for multicast and unicast DA addresses
  - Option to pass all multi-cast addressed packets
  - Promiscuous mode to pass all packets without any filtering for network monitoring
  - Passing of all incoming packets (according to filter) with a status report
- Additional packet filtering that is based on
  - Virtual local area network (VLAN) tag: perfect match and hash-based filtering, which is based on either outer or inner VLAN tag, is possible
  - Layer 3 and layer 4: TCP or UDP over IPv4 or IPv6
  - Extended VLAN tag: filtering based on four filter selections

4.7.8 Serial Audio Interface (SAI)

- Transmitter and receiver has independent bit clock and frame sync
- Transmitter and receiver support up to 4 data lines
- The word size is from 8 to 32 bit. The first word size can be set sperately from other words.
- The maximum frame size is 16 words
- Each transmit and receive data line has a 8 x 32 bit FIFO
  - Automatic graceful restart after FIFO error
  - Support packing 8-bit and 16-bit data into 32-bit FIFO word
  - Support combining FIFOs of multiple data lines into single data line FIFO
- Asynchronous interrupt for both transmitter and receiver, these interrupt source are supported
  - Word start interrupt
  - Sync error interrupt
  - FIFO error, warning and request interrupt
- Support DMA
  - Each data lines has independent DMA enable and DMA request
  - Two DMA request sources, FIFO warning and FIFO request

4.8 Human Machine Interface

4.8.1 General Purpose Input/Output (GPIO)

- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- Inversion for data inputs
- Interrupt flag and enable registers for each pin
- Support for edge sensitive (rising, falling, both) or level sensitive (low, high)
- Asynchronous wake-up in low-power modes
- Pin interrupt is functional in all digital pin muxing modes
- Support getting state of the port in all digital pin muxing modes

4.8.2 Port Controller (PCTRL)

- Individual pull control fields with pullup, pulldown, and pull-disable support
- Individual slew rate field supporting fast and slow slew rates
- Individual input passive filter field supporting enable and disable of the individual input passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to 6 chip-specific digital functions

- Individual digital filter for data inputs
- Individual lock function to avoid misoperation

5 Ordering Information

The following chips are available for ordering.

Table 1: Ordering Table

Product	Memory			Package		IO and ADC channel		Communication
Part number	Flash (MB)	OCRAM (KB)	TCM (KB)	Pin count	Package	GPIOs (Normal)	ADC channels	FlexCAN
YTM32B1HA01G0MLUT	2.25	256	160	176	LQFP	154	64	8
YTM32B1HA01G0MLQT	2.25	256	160	144	LQFP	126	63	8
YTM32B1HA01G0MLLT	2.25	256	160	100	LQFP	87	47	6

5.1 Part Number Information

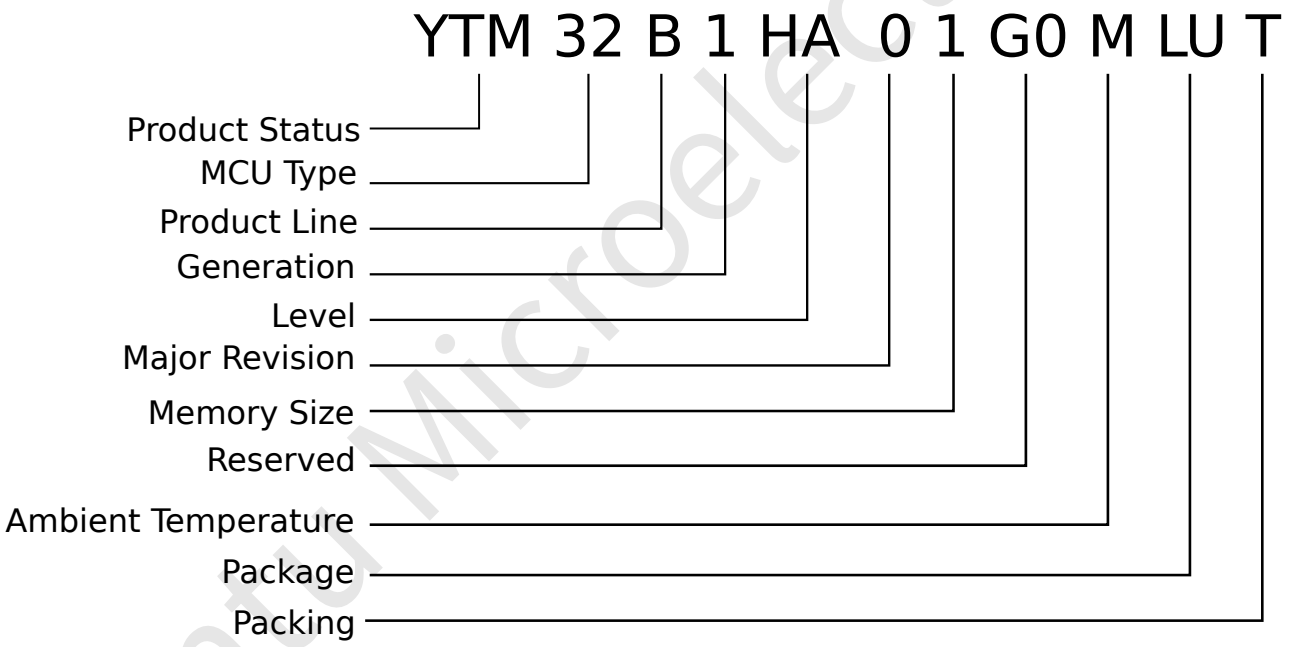


Figure 2: Part Numbers Field

Table 2: Part Number Field Description

Field	Description	Values					
YTM	Product Status	YTM: Qualified PTM: Prototype					
32	MCU Type	32: 32-bit					
B	Product Line	B: General D: Dashboard P: Powertrain V: Vision N: Network					
1	Generation	1st generation product					
HA	Level	Hx: High end Mx: Middle end Lx: Low end					
0	Major Revision	1st revision					
1	Memory Size		1	2	3	4	5
		H	2M	4M	6M	8M	-
		M	64K	128K	256K	512K	1M
		L	8K	16K	32K	64K	128K
G0	Reserved	Reserved					
M	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C					
LU	Package	Pins	LQFP		QFN	BGA	
		32	LE		FM	-	
		48	LF		-	-	
		64	LH		-	-	
		100	LL		-	MH	
		144	LQ		-	-	
		176	LU		-	-	
		205	-		-	MK	
		257	-		-	MM	
		289	-		-	MQ	
T[1]	Packing	T: Trays/Tubes R: Tape and Reel					

1. The chip mark will not contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Patameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ C-Grade\ Part}$	Ambient temperature under bias	-40	–	85	°C
$T_{J\ C-Grade\ Part}$	Junction temperature under bias	-40	–	105	°C
$T_{A\ V-Grade\ Part}$	Ambient temperature under bias	-40	–	105	°C
$T_{J\ V-Grade\ Part}$	Junction temperature under bias	-40	–	125	°C
$T_{A\ M-Grade\ Part}$	Ambient temperature under bias	-40	–	125	°C
$T_{J\ M-Grade\ Part}$	Junction temperature under bias	-40	–	150	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	-500	500	V	
	Corner pins only	-750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	-100	100	mA	3
	Latch-up current at ambient temperature of 25 °C	-200	200	mA	

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

6.2 DC Characteristics

6.2.1 Absolute Maximum Ratings

Table 6: Absolute Maximum Ratings for YTM32B1HA0x Series

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	-0.3	5.8	V	
I_{VDD}	Maximum current into V_{DD}	–	500	mA	
V_{IO}	Digital/Analog IO Input voltage	-0.3	V_{DD} + 0.3	V	
I_O	Instantaneous maximum current of single pin	-25	25	mA	
V_{DDA}	Analog supply voltage	V_{DD} - 0.3	V_{DD} + 0.3	V	

NOTE:

- The maximum ratings are the limits to which the device can be subjected without permanently damaging the device.
- The device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2.2 Voltage and Current Operating Requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.97	5.5	V	
V_{DDA}	Analog supply voltage	2.97	5.5	V	
$V_{DD} - V_{DDA}$	V_{DD} to V_{DDA} differential voltage	-0.1	0.1	V	
I_{ICIO}	DC injection current - single pin				
	$V_{IN} < V_{SS}$ - 0.3V (Negative current injection)	-3	–	mA	1
	$V_{IN} < V_{SS}$ + 0.3V (Negative current injection)	–	3	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive rejection currents of 16 contiguous pins	-25	25	mA	

1. All pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{SS} – 0.3V or greater than V_{DD} + 0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{SS}–0.3V–V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R = [V_{IN}–(V_{DD} + 0.3V)]/|I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.

6.2.3 DC Electrical Specifications at 3.3V

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	2.97	3.3	4.0	V	
V_{ih}	Input buffer high voltage	0.7 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.3 * V_{DD}	V	

Table 8 continued from previous page

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	7	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	–	8	–	mA	
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	11	–	mA	
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	–	13	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	2	–	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	445	–	nA	
V_{OH}	Output high voltage					
	Normal drive pad ($2.97V \leq V_{DD} \leq 4.0V$, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	–	V	
V_{OL}	Output low voltage					
	Normal drive pad ($2.97V \leq V_{DD} \leq 4.0V$, I_{OL} = -2.8mA)	–	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	–	0.002	–	μA	
R_{PU}	Internal pull-up resistors	20	–	100	kΩ	
R_{PD}	Internal pull-down resistors	20	–	105	kΩ	

6.2.4 DC Electrical Specifications at 5.0V

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	4	5	5.5	V	
V_{ih}	Input buffer high voltage	0.65 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.35 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	10	–	mA	

Table 9 continued from previous page

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	–	11	–	mA	
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	15	–	mA	
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	–	16	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	4	–	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	580	–	nA	
V_{OH}	Output high voltage					
	Normal drive pad (2.97V $\leq V_{DD} \leq$ 4.0V, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	–	V	
V_{OL}	Output low voltage					
	Normal drive pad (2.97V $\leq V_{DD} \leq$ 4.0V, I_{OL} = -2.8mA)	–	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	–	0.005	0.5	μA	
R_{PU}	Internal pull-up resistors	20	–	70	kΩ	
R_{PD}	Internal pull-down resistors	20	–	70	kΩ	

6.2.5 Power and Ground Pins

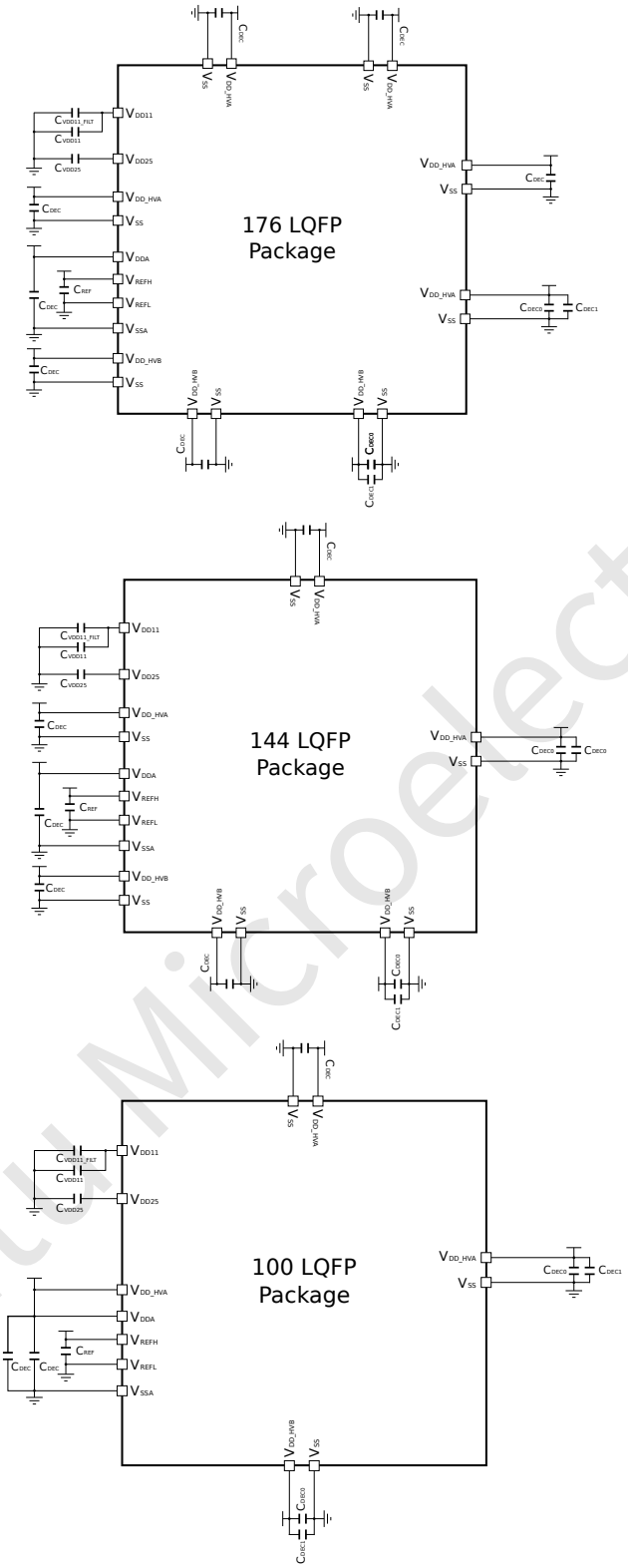


Figure 3: Pinout Decoupling

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF}[1,2]	ADC reference high decoupling capacitance	–	100	–	nF
C_{DEC0}[2,3]	Recommended decoupling capacitance	1	4.7	–	μF
C_{DEC1}[2,3]	Recommended decoupling capacitance	–	0.1	–	μF
C_{VDD11}	Internal PMC, LDO voltage	–	2.2	–	μF
C_{VDD11_FILT}	Internal PMC, LDO voltage, ripple filter	–	100	–	nF
C_{VDD25}	Internal PMC, LDO voltage	–	220	–	nF

1. For improved ADC performance it is recommended to use 1 nF X7R/C0G and 10 nF X7R ceramics in parallel.
2. The capacitors should be placed as close as possible to the VREFH/VREFL pins or corresponding VDD/VSS pins.
3. The requirement and value of of CDEC will be decided by the device application requirement.

6.2.6 POR, LVR and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	–	2.0	–	V	
V_{LVD}	Falling low-voltage threshold	2.7	–	2.9	V	
V_{LVD_HYST}	LVD hysteresis	–	20	–	mV	

6.2.7 Power Mode Transition Operating Behaviors

Description	System clock	Frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	FIRC	96MHz	–	1.2μs	–
DEEPSLEEP -> ACTIVE	FIRC	96MHz	–	22μs	–
STANDBY -> ACTIVE	FIRC	96MHz	–	73μs	–
POWERDOWN -> ACTIVE	FIRC	96MHz	–	240μs	–
T_{POR}	FIRC(reset value)	48MHz	–	2.3ms	–

6.2.8 Power Consumption

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
ACTIVE	I_{DD_ACTIVE}	FIRC	Running coremark in flash, all peripheral clock enabled. core @96MHz, bus @48MHz V_{DD}=5V	25 °C	–	60.5	–	mA
				125 °C	–	87.8	–	mA
			Running coremark in flash, all peripheral clock disabled. core @96MHz, bus @48MHz V_{DD}=5V	25 °C	–	32.7	–	mA
				125 °C	–	58.2	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @96MHz, bus @48MHz V_{DD}=5V	25 °C	–	55.0	–	mA
				125 °C	–	81.4	–	mA

Table 13 continued from previous page

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
			Running while(1) loop in flash, all peripheral clock disabled. core @96MHz, bus @48MHz V_{DD}=5V	25 °C	–	27.0	–	mA
				125 °C	–	52.3	–	mA
		FXOSC	Running coremark in flash, all peripheral clock enabled. core @24MHz, bus @12MHz V_{DD}=5V	25 °C	–	34.9	–	mA
				125 °C	–	59.8	–	mA
			Running coremark in flash, all peripheral clock disabled. core @24MHz, bus @12MHz V_{DD}=5V	25 °C	–	14.0	–	mA
				125 °C	–	38.0	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @24MHz, bus @12MHz V_{DD}=5V	25 °C	–	33.4	–	mA
				125 °C	–	58.2	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @24MHz, bus @12MHz V_{DD}=5V	25 °C	–	12.6	–	mA
				125 °C	–	36.3	–	mA
		PLL	Running coremark in flash, all peripheral clock enabled. core @200MHz V_{DD}=5V	25 °C	–	95.8	–	mA
				125 °C	–	126.5	–	mA
			Running coremark in flash, all peripheral clock disabled. core @200MHz V_{DD}=5V	25 °C	–	59.0	–	mA
				125 °C	–	86.8	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @200MHz V_{DD}=5V	25 °C	–	85.8	–	mA
				125 °C	–	114.1	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @200MHz V_{DD}=5V	25 °C	–	47.7	–	mA
				125 °C	–	74.7	–	mA
			Running while(1) loop in sram, all peripheral clock enabled. core @200MHz V_{DD}=5V	25 °C	–	85.9	–	mA
				125 °C	–	114.2	–	mA
			Running while(1) loop in sram, all peripheral clock disabled. core @200MHz V_{DD}=5V	25 °C	–	47.8	–	mA
				125 °C	–	74.7	–	mA
SLEEP	I_{DD_SLEEP}	PLL	Sleep mode current, V_{DD}=5V Core Frequency @200MHz SIRC, SXOSC enable	$\leq$ 25 °C	–	35.7	–	mA
				125 °C	–	64.0	–	mA
DEEPSLEEP	$I_{DD\_DEEPSLEEP}$	PLL	Deepsleep mode current, V_{DD}=5V SIRC enable, SXOSC disable	$\leq$ 25 °C	–	2.6	–	mA
				125 °C	–	27.8	–	mA
			Deepsleep mode current, V_{DD}=5V SIRC disable, SXOSC enable	$\leq$ 25 °C	–	2.5	–	mA
				125 °C	–	27.6	–	mA
			Deepsleep mode current, V_{DD}=5V SIRC, SXOSC disable	$\leq$ 25 °C	–	2.5	–	mA
				125 °C	–	27.5	–	mA
STANDBY	$I_{DD\_STANDBY}$	PLL	Standby mode current, V_{DD}=5V SIRC enable, SXOSC disable	$\leq$ 25 °C	–	868.8	–	μA
				125 °C	–	22.5	–	mA
			Standby mode current, V_{DD}=5V SIRC disable, SXOSC enable	$\leq$ 25 °C	–	735.4	–	μA
				125 °C	–	22.5	–	mA
			Standby mode current, V_{DD}=5V SIRC and SXOSC disable	$\leq$ 25 °C	–	679.0	–	μA
				125 °C	–	19.1	–	mA

Table 13 continued from previous page

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
POWERDOWN	$I_{DD\_POWERDOWN}$	PLL	Powerdown mode current, V_{DD}=5V SIRC enable, SXOSC disable	$\leq$ 25 °C	–	131.2	–	μA
				125 °C	–	836.7	–	μA
			Powerdown mode current, V_{DD}=5V SIRC disable, SXOSC enable	$\leq$ 25 °C	–	86.7	–	μA
				125 °C	–	788.6	–	μA
			Powerdown mode current, V_{DD}=5V SIRC, SXOSC disable	$\leq$ 25 °C	–	79.5	–	μA
				125 °C	–	800.3	–	μA

6.2.9 Power Sequence

Hardwares must follow the sequence below to ensure that the chip is powered up properly.

1. VDD_HVA/VDD_HVB must be powered up first.
2. VDDA must be powered up later than or at the same time as VDD_HVA/VDD_HVB.
3. VREFH must be powered up later than or at the same time as VDDA.

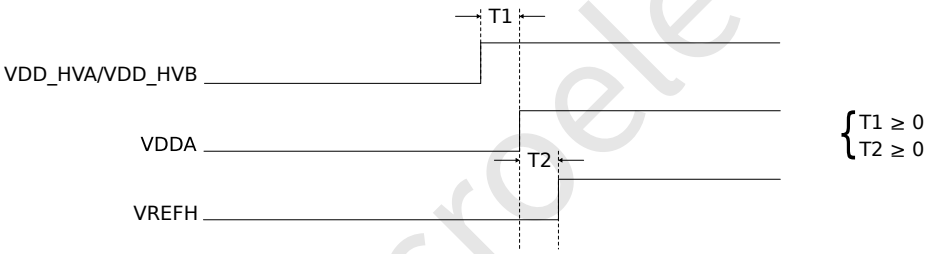


Figure 4: Power Sequence

6.3 AC Characteristics

6.3.1 Device Clock Specifications

Symbol	Description	Min.	Max.	Unit	Notes
f_{core}	System and core clock	–	200	MHz	
f_{fbus}	Fast bus clock	–	100	MHz	
f_{sbus}	Slow bus clock	–	50	MHz	

6.3.2 I/O Electrical Characteristics

6.3.2.1 AC Electrical Characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and the rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

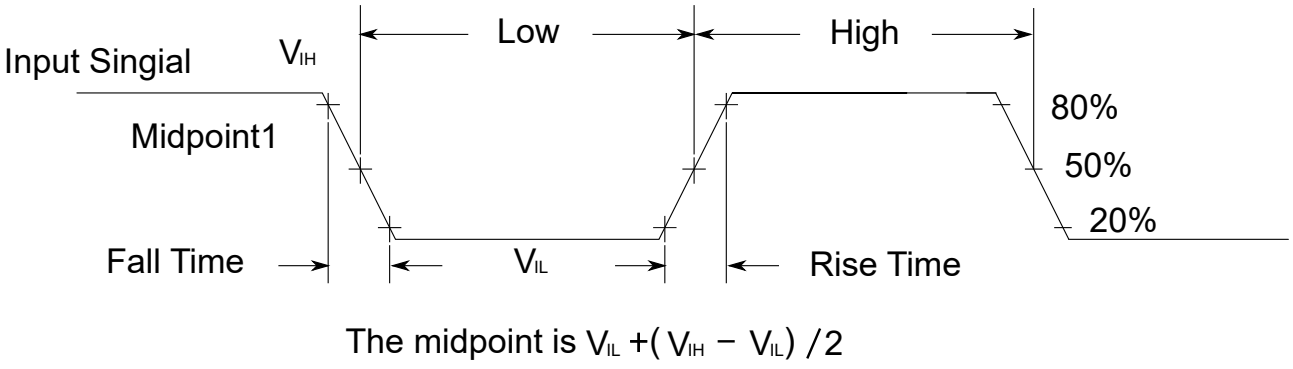


Figure 5: Input Signal Measurement Reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L = 30pF loads
- Normal drive strength

6.4 Peripheral Operating Requirements and Behaviors

6.4.1 FXOSC(4~40 MHz) Characteristics

The following diagram is FXOSC circuit.

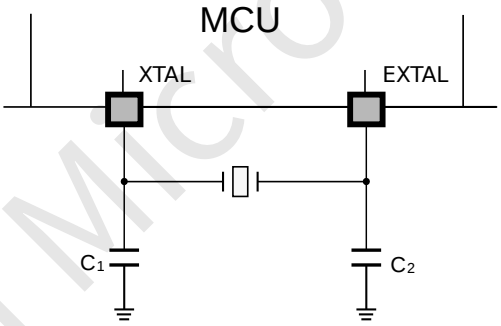


Figure 6: FXOSC Diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDOSC}	FXOSC oscillator	–	0.4	–	mA	
$T_{FXOSCSU}$	FXOSC startup time (24MHz oscillator)	–	0.5	–	ms	
D_{FXOSC}	Duty of FXOSC (24MHz oscillator)	45	–	55	%	
F_{FXOSC}	FXOSC frequency range	4	–	40	MHz	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	FXOSC Internal feedback resistor	–	500	–	KΩ	
V_{PP}	Peak-to-peak amplitude of oscillation (24MHz oscillator)	–	2.25	–	V	

1. Depending on the oscillator manual, $C_L = (C_1 * C_2/(C_1 + C_2)) + C_S$. For crystal load balance, $C_1 = C_2$. C_S is parasitic capacitors, C_L is load capacitor of oscillator, calculate C_1 and C_2 according to this formula.

6.4.2 SXOSC(32.768 KHz) Characteristics

The following diagram is SXOSC circuit.

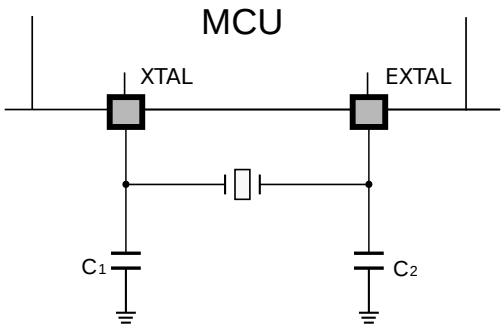


Figure 7: SXOSC Diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SXOSC}	Oscillator crystal frequency	–	32.768	–	KHz	
I_{DDOSC}	SXOSC oscillator	–	6.5	–	μA	
$T_{startup}$	SXOSC startup time (32.768KHz oscillator)	–	–	1	s	
D_{SXOSC}	Duty of SXOSC (32.768KHz oscillator)	47.5	50	52.5	%	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	SXOSC feedback resistor	–	7	–	MΩ	2
V_{PP}	Peak-to-peak amplitude of oscillation (32.768KHz oscillator)	–	2.4	–	V	

1. Depending on the oscillator manual, $C_L = (C_1 * C_2/(C_1 + C_2)) + C_S$. For crystal load balance, $C_1 = C_2$. C_S is parasitic capacitors, C_L is load capacitor of oscillator, calculate C_1 and C_2 according to this formula.
2. The feedback resistor is internal

6.4.3 PLL Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{ref}	PLL reference frequency range	8	–	96	MHz	
F_{input}	PLL input frequency	8	–	48	MHz	5
F_{vco}	VCO frequency	200	–	400	MHz	
F_{out}	Out frequency	100	–	200	MHz	1, 4
N_{pre}	Reference clock predivider divider	1	–	16		2
N_{div}	VCO feedback divider	10	–	64		3

1. PLL OUT divider is 2, $F_{out} = F_{vco}/2$
2. PLL clock pre-divider is from 1 to 16. If need to re-configure. It is recommended to switch to other clock source, then disable PLL, and configure PLL predivider, switch to PLL, and enable it finally.
3. PLL clock feedback divider is from 10 to 63. It is recommended to switch to other clock source, then disable PLL, and configure PLL predivider, switch to PLL, and enable it finally.
4. $F_{out} = \frac{F_{ref}}{2*N_{pre}} * N_{div}$
5. $F_{input} = \frac{F_{ref}}{N_{pre}}$

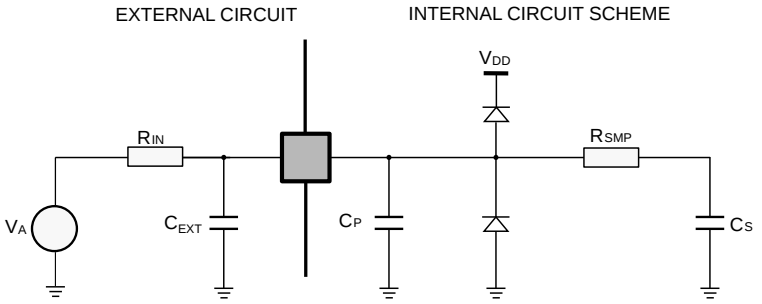
6.4.4 FIRC(96 MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{FIRC}	Fast internal reference frequency	–	96	–	MHz	
ACC_{FIRC}	FIRC frequency accuracy, factory trimmed, 25 °C	-1.0	–	1.0	%	
	FIRC frequency accuracy, factory trimmed, 125 °C	-2.0	–	2.0	%	
I_{FIRC}	FIRC operating current	–	770	–	μA	
$T_{Startup}$	Startup time	–	3	–	μs	

6.4.5 SIRC(12 MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SIRC}	Slow internal reference frequency	–	12	–	MHz	
ACC_{SIRC}	SIRC frequency accuracy, factory trimmed, 125 °C	-2.0	–	2.0	%	
I_{SIRC}	SIRC operating current	–	16	–	μA	
$T_{Startup}$	Startup time	–	10	–	μs	

6.4.6 ADC Characteristics



Note: R_{IN} is the internal resistance of signal source.

Figure 8: ADC Circuit

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage		2.97	5.0	5.5	V	
I_{DDA}	Analog supply current		–	1.25	–	mA	
ΔV_{DDA}	V_{DD} - V_{DDA}		-100	–	100	mV	
V_{REFH}	Reference voltage		2.97	–	V_{DDA}	V	
I_{REFH}	Reference current		–	0.3	–	μA	
V_{IN}	Input voltage		0	–	V_{REFH}	V	
R_{SMP}	Sampling switch impedance		0.18	0.64	1.5	kΩ	
C_{EXT}	External capacitance		–	30	–	nF	
C_P	Pin capacitance		–	3	–	pF	
C_S	Sampling capacitance		–	6.5	–	pF	

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
$T_{STARTUP}$	Analog startup time		–	2	–	μs	
T_{SAMPLE}	Sampling time	ADC functional clock is 32MHz	4	–	–	cycles	
T_{CONV_12BIT}	Total conversion time with sample	ADC functional clock is 32MHz and select 12-bit resolution	–	16	–	cycles	
T_{CONV_10BIT}	Total conversion time with sample	ADC functional clock is 32MHz and select 10-bit resolution	–	14	–	cycles	
T_{CONV_8BIT}	Total conversion time with sample	ADC functional clock is 32MHz and select 8-bit resolution	–	12	–	cycles	
T_{CONV_6BIT}	Total conversion time with sample	ADC functional clock is 32MHz and select 6-bit resolution	–	10	–	cycles	

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
DNL	Differential nonlinear	12-bit resolution	–	$\pm$1.0	–	LSB	
INL	Integer nonlinear	12-bit resolution	–	$\pm$2.0	–	LSB	
E_{GAIN}	Gain error	12-bit resolution	–	2.0	–	LSB	
E_{OFFSET}	Offset error	12-bit resolution	–	1.1	–	LSB	
ENOB	Effective number bits	12-bit resolution	–	10.5	–	Bits	
SINAD	Signal-to-noise-and-distortion ratio	12-bit resolution	–	64.9	–	dB	

6.4.7 ACMP Characteristics

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{ACMP}[1]	Analog supply voltage		2.97	5.0	5.5	V	
$I_{ACMP\_Low\_Power}$	Analog supply current in low power mode		–	69.8	–	μA	
$I_{ACMP\_High\_Speed}$	Analog supply current in high speed mode		–	152.0	–	μA	
$V_{INOFFSET}$	Analog input offset voltage		5.4	–	7.6	mV	
V_{IN}	Analog input voltage		0	–	V_{ACMP}	V	
V_{HYST0}	Analog comparator hysteresis 0		–	10	–	mV	
V_{HYST1}	Analog comparator hysteresis 1		–	16	–	mV	

1. ACMP connects to VDD.

6.4.8 NVM Specifications

6.4.8.1 Flash Timing Specifications - Commands

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
PFlash T_{pgm_256}	PFlash program execution time	–	82.66	85.66	μs	
DFlash T_{pgm_64}	DFlash program execution time	–	50.2	53.2	μs	
T_{sector_erase}	Sector erase execution time	–	16.09	20.09	ms	
T_{block_erase}	Block erase execution time	–	16.06	20.06	ms	
T_{chip_erase}	Chip erase execution time	–	16.06	20.06	ms	
T_{erase_retry}	Erase retry execution time	–	860.28	1060.28	μs	1

1. T_{erase_retry} is sector erase time of each erase retry pulse or pre-erase pulse. It doesn't contain Verify Read time.

6.4.8.2 Reliability Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{nvmretp10k}$	Data retention after up to 10K cycles	5	50	–	years	
$t_{nvmretp1k}$	Data retention after up to 1K cycles	20	100	–	years	
$t_{nvmcycp}$	Cycling endurance	100,000	–	–	cycles	

6.4.9 Debug Module Electrical

6.4.9.1 SWD Electrical Specifications

Table 26: SWD Full Voltage Range Electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

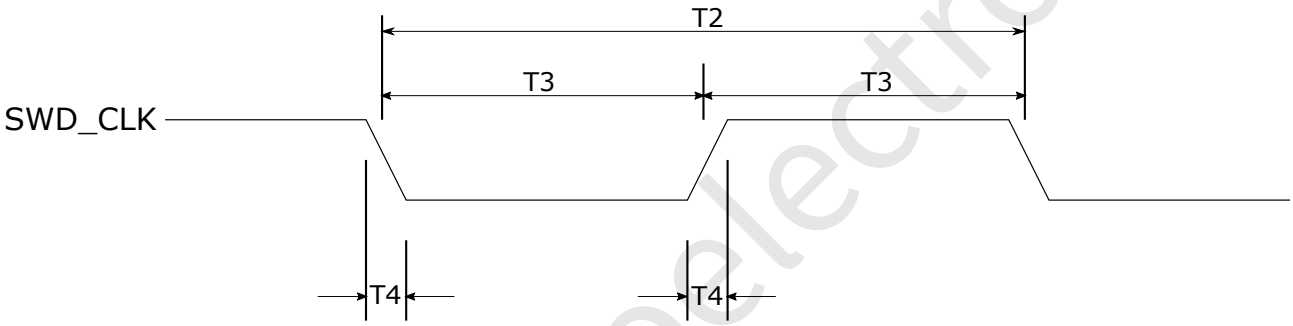


Figure 9: SWD Clock Timing

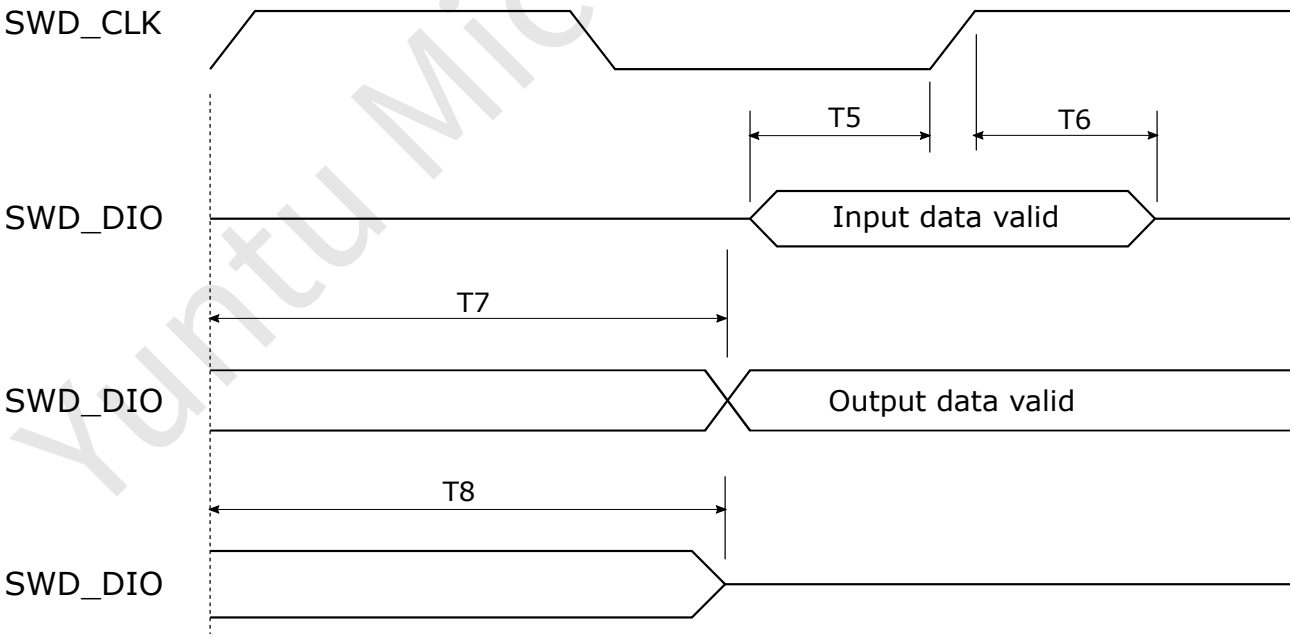


Figure 10: SWD Data Timing

6.4.9.2 JTAG Electrical Specifications

Table 27: JTAG Electrical Specifications

Symbol	Description	Active				Unit
		5.0V IO		3.3V IO		
		Min.	Max.	Min.	Max.	
J1	TCLK frequency					MHz
	Boundary Scan	–	20	–	20	
	JTAG	–	20	–	20	
J2	TCLK cycle period	1/J1	–	1/J1	–	ns
J3	TCLK clock pulse width					ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG					
J4	TCLK rise and fall times	–	1	–	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	–	5	–	ns
J6	Boundary scan input data hold time after TCLK rise	5	–	5	–	ns
J7	TCLK low to boundary scan output data valid	–	28	–	32	ns
J8	TCLK low to boundary scan output data invalid	0	–	0	–	ns
J9	TCLK low to boundary scan output high-Z	–	28	–	32	ns
J10	TMS, TDI input data setup time to TCLK rise	3	–	3	–	ns
J11	TMS, TDI input data hold time after TCLK rise	2	–	2	–	ns
J12	TCLK low to TDO data valid	–	28	–	32	ns
J13	TCLK low to TDO data invalid	0	–	0	–	ns
J14	TCLK low to TDO high-Z	–	28	–	28	ns

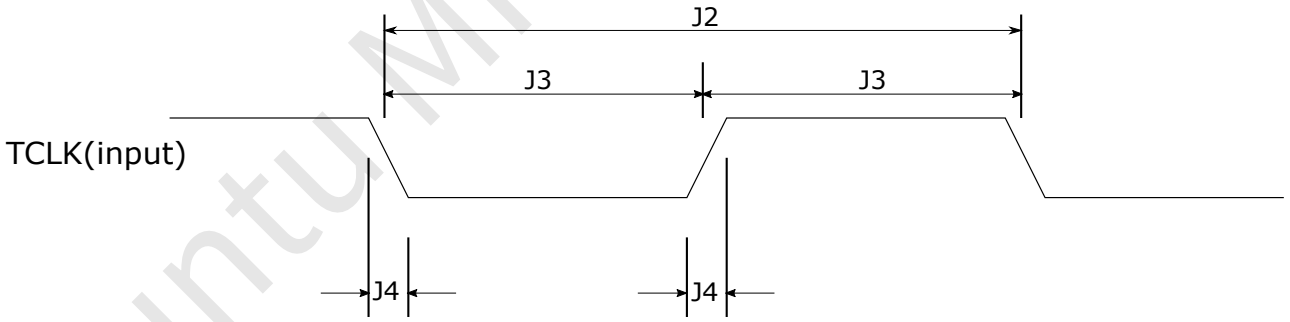


Figure 11: JTAG Clock Timing

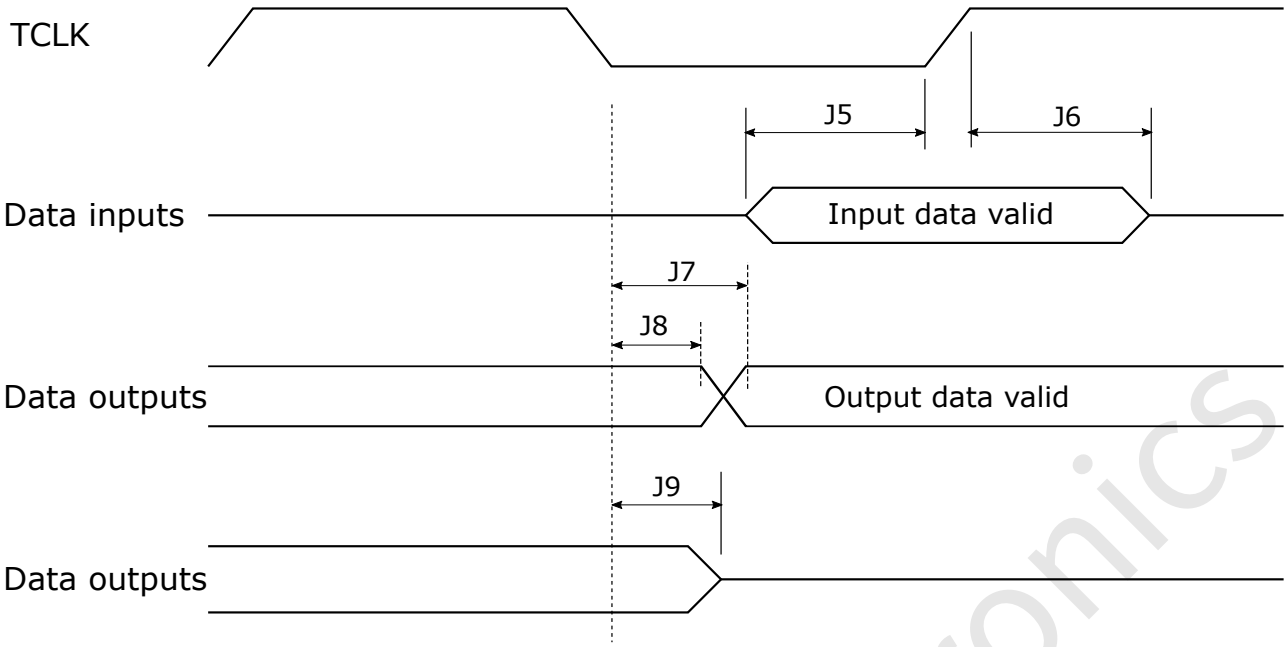


Figure 12: JTAG Data Timing

6.4.10 QSPI Timing

Table 28: QSPI SDR 100MHz

Symbol	Description	Min.	Typ.	Max.	Unit
f_{SCK}	SCK clock frequency	–	–	100	MHz
t_{SCK}	SCK clock period	$1/f_{SCK}$	–	–	μs
t_{SDC}	SCK duty cycle	45	–	55	%
t_{OD}	Data output delay	0.7	–	3.5	ns
t_{ID}	Data input delay	–	–	15	ns
t_{CSSCK}	CS to SCK time	0	–	15 x t_{SCK}	ns
t_{SCKCS}	SCK to CS time	0	–	15 x t_{SCK}	ns

Table 29: QSPI DDR 50MHz

Symbol	Description	Min.	Typ.	Max.	Unit
f_{SCK}	SCK clock frequency	–	–	50	MHz
t_{SCK}	SCK clock period	$1/f_{SCK}$	–	–	μs
t_{SDC}	SCK duty cycle	45	–	55	%
t_{OD}	Data output delay	5.5	–	8.5	ns
t_{ID}	Data input delay	–	–	15	ns
t_{CSSCK}	CS to SCK time	0	–	15 x t_{SCK}	ns
t_{SCKCS}	SCK to CS time	0	–	15 x t_{SCK}	ns

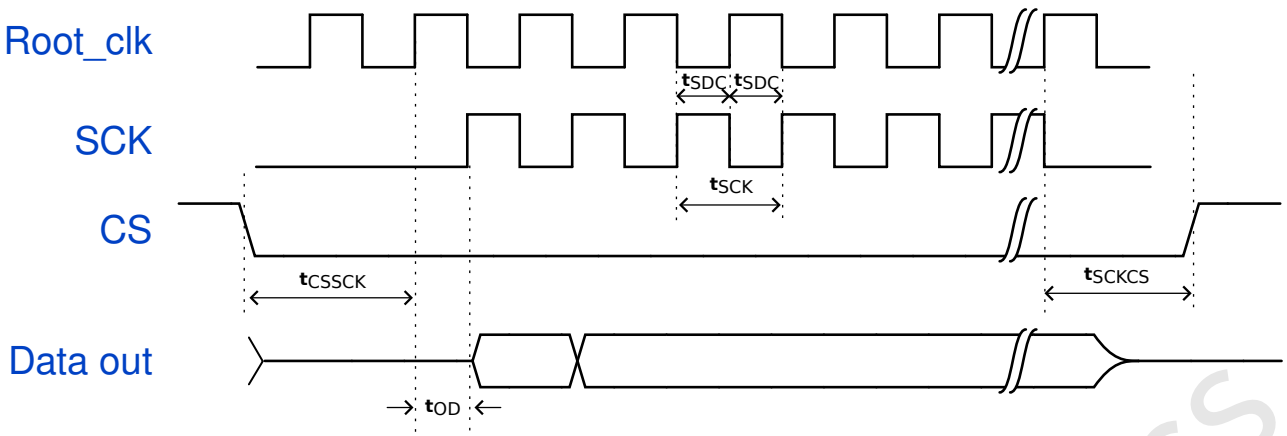


Figure 13: QSPI Output Timing

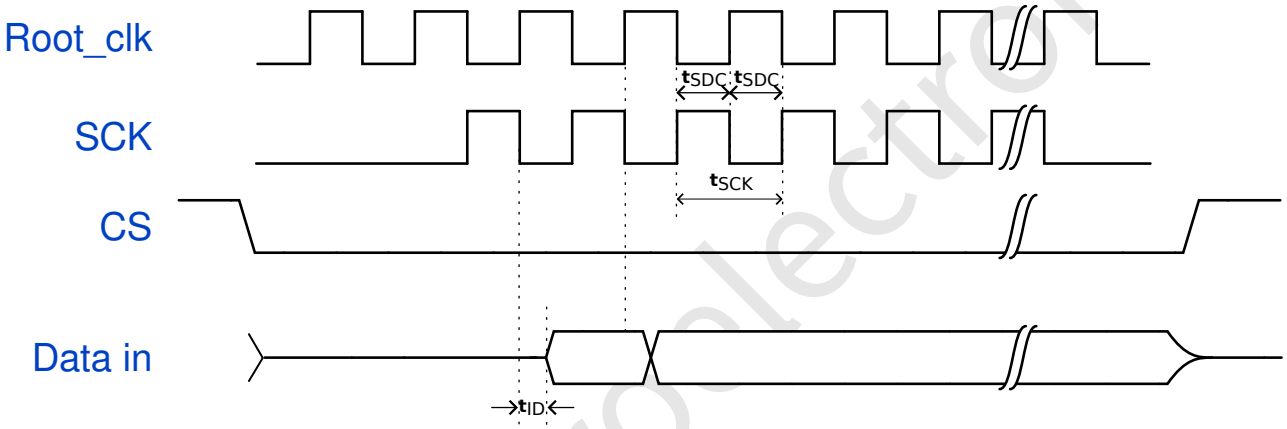


Figure 14: QSPI Input Timing

6.5 Thermal Attributes

Table 30: Thermal Characteristics

Package Family	Package Type	Thermal Resistance JA (°C/W)
LQFP	LQFP100L	57
	LQFP144L	45
	LQFP176L	43

7 Pinouts

7.1 IO Signal Description

The pinouts signal description is as follows:

Table 31: Pinmux Table

100 LQFP	144 LQFP	176 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
		1	PTA_18		PTA_18	eTMR4_CH0	LINFlexD1_TX	SPI1_SOUT	eTMR5_CH0				SPI6_SOUT					MPWM2_CH0	
		2	PTA_19		PTA_19	eTMR4_CH1	LINFlexD1_RX	SPI1_SCK					SPI6_SCK					MPWM2_CH1	
		3	PTA_20		PTA_20	eTMR4_CH2		SPI1_SIN					SPI6_SIN					MPWM2_CH2	
1	1	4	PTE_16	ADC0_S28	PTE_16	LINFlexD3_TX	SPI2_SIN	eTMR2_CH7	eTMR4_FLT0		TMU_OUT7	FMU_ERR_OUT1	SPI6_PCS0					MPWM2_CH3	FMU_ERR_IN1
2	2	5	PTE_15	ADC0_S27	PTE_15	LINFlexD3_RX	SPI2_SCK	eTMR2_CH6	eTMR4_FLT1		TMU_OUT6	FMU_ERR_OUT0	SPI6_PCS1	ACMP1_ACTIVE				MPWM2_CH4	FMU_ERR_IN0
		6	PTA_21		PTA_21	eTMR4_CH3		SPI1_PCS0				SPI2_PCS2	SPI6_PCS2					MPWM2_CH5	
3	3	7	VDD11	VDD11															
4	4	8	VDD25	VDD25															
		9	PTA_22		PTA_22	eTMR4_CH4		SPI1_PCS1					SPI6_PCS3					MPWM2_CH7	
5	5	10	PTE_11	ADC0_S30	PTE_11	SPI2_PCS0	LPTMR0_ALT1	eTMR2_CH5	LINFlexD3_TX	ETM_TRACE_D0	TMU_OUT5	LINFlexD4_TX					SENT1_RX_IN0	MPWM2_CH8	
6	6	11	PTE_10	ADC0_S29	PTE_10	SCU_CLKOUT	SPI2_PCS1	eTMR2_CH4	LINFlexD3_RX		TMU_OUT4	LINFlexD4_RX		SPI3_SIN			SENT1_RX_IN1	MPWM2_CH9	
7	7	12	PTE_13		PTE_13	eTMR4_CH5	SPI2_PCS2	eTMR2_FLT0	SPI2_PCS0							eTMR3_CH5	SENT1_RX_IN2	MPWM2_CH10	
		13	PTA_23		PTA_23	eTMR4_CH6												MPWM2_CH11	
8	8	14	PTE_5		PTE_5	TCLK_IN2	eTMR2_QD_PHA	eTMR2_CH3	CAN0_TX	eTMR3_CH5							SENT1_RX_IN3	MPWM2_CH12	
9	9	15	PTE_4		PTE_4	ETM_TRACE_D1	eTMR2_QD_PHB	eTMR2_CH2	CAN0_RX	eTMR3_CH4		SPI0_PCS0	eTMR3_CH7		SPI1_PCS1			MPWM2_CH13	
		16	PTA_24		PTA_24	eTMR4_CH7								eTMR4_CH0				MPWM2_CH14	
	10	17	PTA_25		PTA_25	eTMR5_CH0												MPWM2_CH15	
10	11	18	VDD_HVA	VDD_HVA															
	12	19	VSS	VSS															
11	13	20	VDDA	VDDA															
12	14	21	VREFH	VREFH															
13	15	22	VREFL	VREFL															
14	16	23	VSSA	VSSA															
15	17	24	PTB_7	EXTAL	PTB_7	I2C0_SCL		SPI3_SCK	eTMR4_FLT3		TMU_OUT2								
16	18	25	PTB_6	XTAL	PTB_6	I2C0_SDA		SPI3_SIN	eTMR4_FLT2		TMU_OUT1								
	19	26	PTA_26		PTA_26	eTMR5_CH1	SPI1_PCS0	SPI0_PCS0			ENET_PPS0			eTMR4_CH1					
17	20	27	PTE_14		PTE_14	eTMR0_FLT1		eTMR2_FLT1			ENET_PPS1	CAN4_RX			eTMR2_CH3	LINFlexD5_TX			
18	21	28	PTE_3		PTE_3	eTMR0_FLT0	SPI1_SIN	eTMR2_FLT0	SPI3_SOUT	TMU_IN6	ACMP0_OUT	CAN4_TX	eTMR2_CH3		ENET_PPS0	LINFlexD5_RX			
	22	29	PTA_27		PTA_27	eTMR5_CH2	SPI1_SOUT	LINFlexD0_TX	CAN0_TX				ENET_PPS1		eTMR4_CH2				
19	23	30	PTE_12	DAC1_OUT	PTE_12	eTMR0_FLT3	LINFlexD2_TX	eTMR5_FLT0	SPI3_PCS0				eTMR3_CH5	ENET_PPS3		CAN5_TX			
	24	31	PTA_28		PTA_28	eTMR5_CH3	SPI1_SCK	LINFlexD0_RX	CAN0_RX					eTMR4_CH3					
20	25	32	PTD_17		PTD_17	eTMR0_FLT2	LINFlexD2_RX	eTMR5_FLT1	SPI3_PCS0		ENET_PPS2		SPI5_PCS0		CAN5_RX	eTMR2_CH2	ENET_MII_ RMII_MDC		
	26	33	PTA_29		PTA_29	eTMR5_CH4		LINFlexD2_TX	SPI1_SIN				ENET_PPS2	eTMR4_CH4					
	27	34	PTA_30		PTA_30	eTMR5_CH5	LINFlexD2_RX	SPI0_SOUT						eTMR4_CH5	SPI1_SOUT				
21	28	35	PTD_16	EXTAL32	PTD_16	eTMR0_CH1	CAN4_TX	SPI0_SIN	ACMP0_ACTIVE	ETM_TRACE_D2	ETM_TRACE_ CLKOUT		eTMR4_CH7		LINFlexD8_TX		ENET_MII_ RMII_MDIO		
22	29	36	PTD_15	XTAL32	PTD_15	eTMR0_CH0	CAN4_RX	SPI0_SCK	SPI3_PCS1	ETM_TRACE_D3	LINFlexD8_RX	SAI1_SYNC	ENET_PPS2		CAN3_RX	eTMR4_CH6			
23	30	37	PTE_9		PTE_9	eTMR0_CH7	SPI1_SCK	I2C2_SDA	ENET_PPS3	ENET_MII_ RMII_TX_EN		SPI5_SOUT			CAN3_TX	eTMR4_CH5			
	31	38	VSS	VSS															
	32	39	VDD_HVB	VDD_HVB															
	33	40	PTA_31		PTA_31	eTMR5_CH6		SPI0_PCS1			TMU_OUT8			eTMR4_CH6				MPWM0_CH4	
24	34	41	PTD_14		PTD_14	eTMR2_CH5	LINFlexD1_TX	I2C0_SCL	ENET_PPS0	SAI1_MCLK		SPI5_SCK	SPI5_PCS3	SCU_CLKOUT	ACMP0_ACTIVE			MPWM2_CH6	
25	35	42	PTD_13		PTD_13	eTMR2_CH4	LINFlexD1_RX	I2C0_SDA	ENET_PPS1	SAI1_DATA0	RTC_CLKOUT	SPI5_SIN	SPI5_PCS2					MPWM0_CH5	
	36	43	PTB_18	ADC0_S16	PTB_18	eTMR5_CH7		SPI1_PCS1			TMU_OUT9	LINFlexD2_TX		eTMR4_CH7				MPWM0_CH6	
		44	PTB_19		PTB_19	eTMR4_CH7				eTMR5_CH7	TMU_OUT10	LINFlexD2_RX					QSPI_DQSA		
	37	45	PTB_20	ADC0_S17	PTB_20	LINFlexD3_TX			I2C1_SDA						eTMR5_CH0		QSPI_IOFA[4]		
	38	46	PTB_21	ADC0_S18	PTB_21	LINFlexD3_RX			I2C1_SCL						eTMR5_CH1		QSPI_IOFA[5]		
26	39	47	PTE_8	ACMP0_IN3	PTE_8	eTMR0_CH6	SPI5_PCS1	I2C2_SCL	ENET_MII_ RMII_MDC	SAI1_BCLK		SPI3_PCS1				SENT0_RX_IN0	QSPI_IOFA[6]		

Table 31 continued from previous page

100 LQFP	144 LQFP	176 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
27	40	48	PTB_5		PTB_5	eTMR0_CH5	SPI0_PCS1	SPI0_PCS0		TMU_IN0	ENET_MII_ RMII_MDC	ENET_MII_ RMII_TXD[0]	eTMR4_CH3	I2C2_SCL		SENT0_RX_IN1	QSPI_IOFA[7]		
28	41	49	PTB_4		PTB_4	eTMR0_CH4	SPI0_SOUT			TMU_IN1	ENET_MII_ RMII_MDIO	ENET_MII_ RMII_TXD[1]	eTMR4_CH2	SCU_CLKOUT		SENT0_RX_IN2			QSPI_IOFB[0]
29	42	50	PTC_3	ADC0_S11/ ACMP0_IN4	PTC_3	eTMR0_CH3	CAN0_TX	LINFlexD0_TX	SPI4_PCS0	QSPI_PCSFA						SENT0_RX_IN3			QSPI_IOFB[3]
30	43	51	PTC_2	ADC0_S10/ ACMP0_IN5	PTC_2	eTMR0_CH2	CAN0_RX	LINFlexD0_RX	SPI4_SCK	ETM_TRACE_ CLKOUT	QSPI_IOFA[3]	ENET_MII_ RMII_TXD[1]	SPI0_PCS2	SPI3_PCS2	ENET_MII_ RMII_TXD[0]				
31	44	52	PTD_7	ACMP0_IN6	PTD_7	LINFlexD2_TX	eTMR0_CH3	eTMR2_FLT3	SPI4_SIN	ETM_TRACE_D0	QSPI_IOFA[1]	ENET_MII_ RMII_TXD[0]			SPI3_PCS3	SPI0_PCS3	ENET_MII_ RMII_TXD[1]		
32	45	53	PTD_6	ACMP0_IN7	PTD_6	LINFlexD2_RX	eTMR0_CH2	eTMR2_FLT2	SPI4_SOUT		SPI0_PCS0	ENET_MII_TXD3	ENET_MII_ RMII_TX_CLK		eTMR4_CH4	ENET_MII_TXD2			QSPI_IOFB[1]
33	46	54	PTD_5		PTD_5	eTMR2_CH3	LPTMR0_ALT2	eTMR2_FLT1	SPI4_PCS1	TMU_IN7	SPI0_PCS1	ENET_MII_TXD2	ENET_MII_ RX_CLK		eTMR0_CH2	ENET_MII_TXD3			QSPI_IOFB[2]
34	47	55	PTD_12		PTD_12	eTMR2_CH2		ETM_TRACE_D1	ENET_MII_ RMII_TX_EN	SPI0_SOUT	QSPI_IOFA[2]		ENET_MII_ RMII_TX_CLK			SPI5_SIN			
35	48	56	PTD_11		PTD_11	eTMR2_CH1	eTMR2_QD_PHA	ETM_TRACE_D2		SPI0_SCK	QSPI_IOFA[0]	ENET_MII_TXD2	ENET_MII_ RMII_TX_CLK		ENET_MII_ RMII_TX_EN		SPI5_SOUT		
36	49	57	PTD_10		PTD_10	eTMR2_CH0	eTMR2_QD_PHB	ETM_TRACE_D3	SPI0_SIN		QSPI_SCKFA	ENET_MII_TXD3	ENET_MII_ RX_CLK		eTMR4_CH2		SPI5_SCK	SCU_CLKOUT	
37	50	58	VSS	VSS															
38	51	59	VDD_HVB	VDD_HVB															
39	52	60	PTC_1	ADC0_S9	PTC_1	eTMR0_CH1	SPI2_SOUT	CAN3_TX		eTMR1_CH7		CAN3_RX	ENET_MII_ RMII_RXD[0]	ENET_MII_ RX_CLK			ENET_MII_ RMII_RXD[1]		QSPI_SCKFB
40	53	61	PTC_0	ADC0_S8	PTC_0	eTMR0_CH0	SPI2_SIN	CAN3_RX		eTMR1_CH6	ENET_MII_ RMII_TX_CLK	CAN3_TX	ENET_MII_ RMII_RXD[1]				ENET_MII_ RMII_RXD[0]		QSPI_DQSB
41	54	62	PTD_9		PTD_9	LINFlexD4_TX		eTMR2_FLT3		eTMR1_CH5			ENET_MII_RXD2	I2C1_SCL	LINFlexD6_TX	FMU_ERR_IN2	ENET_MII_ RMII_RXD[0]		QSPI_IOFB[4]
42	55	63	PTD_8		PTD_8	LINFlexD4_RX		eTMR2_FLT2		eTMR1_CH4		SPI3_SOUT	ENET_MII_RXD3	I2C1_SDA	LINFlexD6_RX	FMU_ERR_IN3	ENET_MII_ RMII_RXD[1]		QSPI_IOFB[5]
43	56	64	PTC_17	ADC0_S15	PTC_17	eTMR1_FLT3	CAN2_TX	SPI4_PCS0	eTMR2_CH1			SPI3_SCK					ENET_MII_ RMII_RX_DV		QSPI_IOFB[6]
44	57	65	PTC_16	ADC0_S14	PTC_16	eTMR1_FLT2	CAN2_RX	SPI4_SCK	eTMR2_CH0		I2C1_SDA	SPI3_SIN	eTMR4_CH1			LINFlexD2_RX	ENET_MII_ RMII_RX_ER		QSPI_IOFB[7]
	58	66	PTB_22	ADC0_S19	PTB_22	eTMR5_CH2	SPI3_PCS1		LINFlexD1_TX			CAN2_RX	ENET_MII_CRS	CAN1_TX					QSPI_IOFB[3]
45	59	67	PTC_15	ADC0_S13	PTC_15	eTMR1_CH3	SPI2_SCK	SPI4_SIN	LINFlexD4_TX	TMU_IN8	I2C1_SCL	CAN2_TX	ENET_MII_CRS	CAN1_RX	LINFlexD2_TX		ENET_MII_ RMII_RX_DV	ENET_MII_RXD2	QSPI_PCSFB
	60	68	PTB_23	ADC0_S20	PTB_23		LINFlexD1_RX				CAN1_RX		ENET_MII_COL	eTMR5_CH3					
		69	PTB_24		PTB_24	eTMR5_CH4					CAN1_TX								
46	61	70	PTC_14	ADC0_S12	PTC_14	eTMR1_CH2	SPI2_PCS0	SPI4_SOUT	LINFlexD4_RX	TMU_IN9	eTMR3_CH4		ENET_MII_COL	CAN2_RX			ENET_MII_ RMII_RX_ER	ENET_MII_RXD3	
	62	71	PTB_25	ADC0_S21	PTB_25			SPI4_PCS1	SPI2_PCS0				eTMR5_CH5	CAN2_TX					
		72	PTB_26		PTB_26	eTMR5_CH6													
47	63	73	PTB_3	ADC0_S7	PTB_3	eTMR1_CH1	SPI0_SIN	eTMR1_QD_PHA	CAN4_TX	TMU_IN2					SPI2_SOUT	SAI0_MCLK			
	64	74	PTB_27	ADC0_S22	PTB_27	eTMR5_FLT2			SPI2_SOUT			LINFlexD5_TX	eTMR5_CH7					MPWM0_CH0	
	65	75	PTB_28	ADC0_S23	PTB_28	eTMR5_FLT3			SPI2_SIN		ENET_PPS3		LINFlexD5_RX					MPWM0_CH1	

Table 31 continued from previous page

100 LQFP	144 LQFP	176 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
	66	76	VSS	VSS															
	67	77	VDD_HVB	VDD_HVB															
48	68	78	PTB_2	ADC0_S6	PTB_2	eTMR1_CH0	SPI0_SCK	eTMR1_QD_PHB		TMU_IN3	SAI0_DATA0		CAN4_RX	LINFlexD9_RX		SPI2_SIN		MPWM0_CH2	
	69	79	PTB_29		PTB_29				SPI2_SCK		SAI0_DATA1	LINFlexD6_TX		LINFlexD9_TX				MPWM0_CH3	
		80	PTB_30		PTB_30													MPWM0_CH4	
49	70	81	PTC_13		PTC_13	eTMR3_CH7	eTMR2_CH7				SAI0_SYNC				eTMR3_CH3				
		82	PTB_31		PTB_31								CAN7_TX					MPWM0_CH5	
		83	PTC_18		PTC_18						SAI0_DATA2	LINFlexD6_RX	CAN7_RX					MPWM0_CH6	
50	71	84	PTC_12		PTC_12	eTMR3_CH6	eTMR2_CH6	SPI2_PCS1			SAI0_BCLK		CAN6_TX		eTMR3_CH2				
	72	85	PTC_19		PTC_19				SPI2_PCS1		SAI0_DATA3	LINFlexD7_TX	CAN6_RX					MPWM0_CH7	
		86	PTC_20		PTC_20							LINFlexD7_RX						MPWM0_CH8	
		87	PTC_21		PTC_21													MPWM0_CH9	
		88	PTC_22		PTC_22							eTMR1_CH0						MPWM0_CH10	
	73	89	PTC_23		PTC_23	SPI0_SCK												MPWM0_CH11	
		90	PTC_24		PTC_24	eTMR4_CH0	eTMR3_CH0						CAN6_TX					MPWM0_CH12	
		91	PTC_25		PTC_25	eTMR4_CH1	eTMR3_CH1		SPI4_PCS1				CAN6_RX					MPWM0_CH13	
51	74	92	PTC_11		PTC_11	eTMR3_CH5	eTMR4_CH2	CAN5_TX		TMU_IN10			CAN5_RX		eTMR3_CH1	SPI4_SOUT			
		93	PTC_26		PTC_26	eTMR4_CH3	eTMR3_CH3				SPI4_SIN		CAN5_RX					MPWM0_CH14	
52	75	94	PTC_10	ADC1_S27	PTC_10	eTMR3_CH4		CAN5_RX	SPI4_PCS0	TMU_IN11	eTMR3_CH0	eTMR0_CH6		CAN5_TX		SPI2_PCS1			
	76	95	PTC_27		PTC_27	eTMR4_CH4					SPI4_SCK	CAN5_TX			eTMR3_CH4			MPWM0_CH15	
53	77	96	PTB_1	ADC0_S5	PTB_1	LINFlexD0_TX	SPI0_SOUT	TCLK_IN0	CAN0_TX	eTMR4_CH5				eTMR3_CH5		eTMR0_CH7		MPWM0_CH0	
54	78	97	PTB_0	ADC0_S4	PTB_0	LINFlexD0_RX	SPI0_PCS0	LPTMR0_ALT3	CAN0_RX	eTMR4_CH6				eTMR3_CH6		eTMR0_CH3		MPWM0_CH1	
	79	98	PTC_28		PTC_28	eTMR4_CH7			I2C1_SCL			CAN3_TX			eTMR3_CH7				
55	80	99	PTC_9		PTC_9	LINFlexD1_TX	eTMR1_FLT1	eTMR5_CH0	CAN4_TX	SPI0_SIN	I2C0_SDA		CAN1_RX	eTMR4_CH0			SPI5_PCS1	MPWM0_CH2	
56	81	100	PTC_8	DAC0_OUT	PTC_8	LINFlexD1_RX	eTMR1_FLT0	eTMR5_CH1	CAN4_RX	SPI0_SCK	I2C0_SCL		CAN1_TX	eTMR4_CH1			SPI5_PCS0	MPWM0_CH3	
	82	101	PTC_29		PTC_29	eTMR5_CH2			I2C1_SDA			CAN3_RX	eTMR4_CH2						
57	83	102	PTA_7	ADC0_S3	PTA_7	eTMR0_FLT2	eTMR5_CH3	RTC_CLKIN	I2C2_SCL			LINFlexD3_TX	SPI0_PCS1	eTMR4_CH3	CAN0_TX			SPI5_SCK	
	84	103	PTC_30		PTC_30	eTMR5_CH4						CAN4_TX	eTMR4_CH4						
58	85	104	PTA_6	ADC0_S2	PTA_6	eTMR0_FLT1	SPI1_PCS1	eTMR5_CH5	I2C2_SDA	SPI3_PCS1		LINFlexD3_RX	CAN0_RX	eTMR4_CH5			SPI5_SIN		
	86	105	PTC_31		PTC_31	eTMR5_CH6		I2C1_SDA					CAN4_RX		eTMR4_CH6				
59	87	106	PTE_7		PTE_7	eTMR0_CH7	eTMR3_FLT0			SPI3_SCK			LINFlexD4_RX		SPI5_SOUT				
	88	107	PTD_18	ADC1_S16	PTD_18	eTMR5_CH7	CAN5_TX	I2C1_SCL	I2C1_SDA				CAN7_TX						
	89	108	PTD_19	ADC1_S17	PTD_19		CAN5_RX		I2C1_SCL				CAN7_RX						
60	90	109	VSS	VSS															
61	91	110	VDD_HVA	VDD_HVA															
62	92	111	PTA_17		PTA_17	eTMR0_CH6	eTMR3_FLT0		eTMR5_FLT0	SPI3_SOUT		LINFlexD4_TX		EWDG_OUT_b				MPWM2_CH0	
63	93	112	PTB_17	ADC1_S26	PTB_17	eTMR0_CH5	SPI1_PCS3	eTMR5_FLT1		SPI3_PCS0		LINFlexD4_RX		eTMR3_CH7				MPWM2_CH1	
		113	PTD_20	ADC1_S31	PTD_20	eTMR5_CH1			SPI1_PCS2	SPI3_SIN									
64	94	114	PTB_16	ADC1_S15	PTB_16	eTMR0_CH4	SPI1_SOUT	LINFlexD4_TX					SENT1_RX_IN0						
65	95	115	PTB_15	ADC1_S14	PTB_15	eTMR0_CH3	SPI1_SIN			LINFlexD7_TX			SENT1_RX_IN1					MPWM2_CH2	
66	96	116	PTB_14	ADC1_S9	PTB_14	eTMR0_CH2	SPI1_SCK			LINFlexD7_RX			SENT1_RX_IN2					MPWM2_CH3	
		117	PTD_21		PTD_21	eTMR5_CH2													
67	97	118	PTB_13	ADC1_S8	PTB_13	eTMR0_CH1	eTMR3_FLT1	CAN2_TX			LINFlexD8_TX	SPI3_PCS2	SENT1_RX_IN3						
68	98	119	PTB_12	ADC1_S7	PTB_12	eTMR0_CH0	eTMR3_FLT2	CAN2_RX			LINFlexD8_RX	SPI3_PCS3							
	99	120	PTD_22	ADC1_S18	PTD_22	eTMR4_FLT2							eTMR5_CH3						
69	100	121	PTD_4	ADC1_S6	PTD_4	eTMR0_FLT3	eTMR3_FLT3				SPI5_PCS0		eTMR5_CH7	SPI1_PCS1		SPI5_PCS2			
70	101	122	PTD_3	ADC1_S3	PTD_3	eTMR3_CH5	SPI1_PCS0	I2C1_SCL	CAN5_TX	TMU_IN4	NMI_b		eTMR5_CH6	LINFlexD3_RX					
71	102	123	PTD_2	ADC1_S2	PTD_2	eTMR3_CH4	SPI1_SOUT	I2C1_SDA	CAN5_RX	TMU_IN5	SPI5_SOUT		eTMR5_CH5	LINFlexD3_TX					
	103	124	PTD_23	ADC1_S19	PTD_23	eTMR4_FLT3							eTMR5_CH4						
72	104	125	PTA_3	ADC1_S1	PTA_3	eTMR3_CH1	I2C0_SCL			LINFlexD0_TX	SPI5_SCK	FMU_ERR_OUT1	eTMR5_CH4	SPI1_SCK					FMU_ERR_IN1
73	105	126	PTA_2	ADC1_S0/ ACMP1_IN2	PTA_2	eTMR3_CH0	I2C0_SDA			LINFlexD0_RX	SPI5_SIN	FMU_ERR_OUT0	eTMR5_CH3				SPI1_SIN		FMU_ERR_IN0
	106	127	PTD_24	ADC1_S20	PTD_24								eTMR5_CH5						
74	107	128	PTB_11	ADC1_S30	PTB_11	eTMR3_CH3	LINFlexD5_TX					SPI4_SIN	eTMR5_CH2						
		129	VDD_HVA	VDD_HVA															

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100 LQFP	144 LQFP	176 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
		130	VSS	VSS															
75	108	131	PTB_10	ADC1_S29	PTB_10	eTMR3_CH2	LINFlexD5_RX	SAI1_MCLK	LINFlexD9_TX			SPI4_SCK	eTMR5_CH1						
		132	PTD_25		PTD_25	eTMR5_CH6													
76	109	133	PTB_9	ADC0_S25	PTB_9	eTMR5_CH0	eTMR3_CH1	SAI1_DATA0	LINFlexD9_RX			SPI4_SOUT							
		134	PTD_26		PTD_26	eTMR5_CH7				SPI5_SCK									
	110	135	PTD_27	ADC1_S21	PTD_27	eTMR5_FLT2				SPI5_SOUT									
77	111	136	PTB_8	ADC0_S24	PTB_8	eTMR3_CH0		SAI1_BCLK		SPI0_PCS5		SPI4_PCS0	eTMR4_CH7						
	112	137	PTD_28	ADC1_S22	PTD_28	eTMR5_FLT3				SPI5_SIN									
78	113	138	PTA_1	ADC0_S1/ ACMP_IN1[1]	PTA_1	eTMR1_CH1	LINFlexD5_TX		eTMR1_QD_PHA	SPI0_PCS6	TMU_OUT0	SPI4_PCS1							
	114	139	PTD_29	ADC1_S23	PTD_29					SPI5_PCS2									
79	115	140	PTA_0	ADC0_S0/ ACMP_IN0[2]	PTA_0	eTMR2_CH1	LINFlexD5_RX		eTMR2_QD_PHA	SPI0_PCS7	TMU_OUT3	SPI4_PCS2		eTMR3_CH0					FMU_ERR_IN2
	116	141	PTD_30		PTD_30					SPI5_PCS3									
		142	PTD_31		PTD_31														
80	117	143	PTC_7	ADC1_S5	PTC_7	LINFlexD1_TX	CAN1_TX	eTMR3_CH3	eTMR3_CH7	eTMR1_QD_PHA		I2C1_SCL		SPI0_PCS0		CAN2_TX			FMU_ERR_IN3
81	118	144	PTC_6	ADC1_S4	PTC_6	LINFlexD1_RX	CAN1_RX	eTMR3_CH2	eTMR3_CH6	eTMR1_QD_PHB		I2C1_SDA		SPI0_PCS1		CAN2_RX	SPI1_PCS1	MPWM1_CH9	
		145	PTE_17		PTE_17														
82	119	146	PTA_16	ADC1_S13	PTA_16	eTMR1_CH3	SPI1_PCS2	SPI0_PCS4	LINFlexD6_TX			SPI4_PCS3						MPWM1_CH0	
		147	PTE_18		PTE_18														
83	120	148	PTA_15	ADC1_S12	PTA_15	eTMR1_CH2	SPI0_PCS3	SPI2_PCS3	LINFlexD6_RX	SPI5_PCS0	SAI0_SYNC							MPWM1_CH1	
84	121	149	PTE_6	ADC1_S11	PTE_6	SPI0_PCS2		eTMR3_CH7		SAI0_DATA1		eTMR4_CH6		ETM_TRACE_D2	ETM_TRACE_ CLKOUT			MPWM1_CH2	
85	122	150	PTE_2	ADC1_S10	PTE_2	SPI0_SOUT	LPTMR0_ALT3	eTMR3_CH6		SAI0_DATA2		eTMR0_CH3	eTMR4_CH0		ETM_TRACE_D3			MPWM1_CH3	
86	123	151	VSS	VSS															
87	124	152	VDD_HVA	VDD_HVA															
	125	153	PTE_19		PTE_19	eTMR2_CH6			I2C4_SDA										
	126	154	PTE_20		PTE_20	eTMR4_CH0			I2C4_SCL				eTMR3_CH0						
88	127	155	PTA_14	ADC1_S28	PTA_14	eTMR0_FLT0	eTMR3_FLT1			eTMR1_FLT0	SAI0_DATA3		eTMR3_CH4	SPI1_PCS3	SPI5_PCS1			MPWM1_CH0	
	128	156	PTE_21		PTE_21	eTMR4_CH1				SPI4_SIN			eTMR3_CH1					MPWM1_CH1	
	129	157	PTE_22		PTE_22	eTMR4_CH2				SPI4_SCK			eTMR3_CH2					MPWM1_CH2	
89	130	158	PTA_13	ADC1_S25	PTA_13	eTMR1_CH7	CAN1_TX	SPI3_PCS0		eTMR2_QD_PHA	SAI0_DATA0	SPI1_PCS4	eTMR3_CH3					MPWM1_CH3	
	131	159	PTE_23		PTE_23	eTMR4_CH3	CAN1_RX			SPI4_PCS0			eTMR3_CH3					MPWM1_CH4	
	132	160	PTE_24		PTE_24	eTMR4_CH4	CAN2_TX			SPI4_PCS1			eTMR3_CH4					MPWM1_CH5	
	133	161	PTE_25		PTE_25	eTMR4_CH5	CAN2_RX			SPI4_SOUT			eTMR3_CH5					MPWM1_CH6	
90	134	162	PTA_12	ADC1_S24	PTA_12	eTMR1_CH6	CAN1_RX	SPI3_SCK		eTMR2_QD_PHB	SAI0_BCLK	ACMP1_OUT	SPI1_PCS5	eTMR3_CH2			SENT0_RX_IN0	MPWM1_CH7	
91	135	163	PTA_11		PTA_11	eTMR1_CH5	CAN1_TX	SPI3_SIN	ACMP0_ACTIVE	SPI1_PCS0			eTMR3_CH1	SPI7_PCS0			SENT0_RX_IN1	MPWM1_CH8	
92	136	164	PTA_10		PTA_10	eTMR1_CH4		SPI3_SOUT									SENT0_RX_IN2		JTAG_TDO SWD_SWO
93	137	165	PTE_1		PTE_1	SPI0_SIN		I2C1_SCL	SPI1_PCS0	eTMR1_FLT1			SPI0_SCK	SPI7_SIN	LINFlexD7_TX		SENT0_RX_IN3	MPWM1_CH10	
94	138	166	PTE_0		PTE_0	SPI0_SCK	TCLK_IN1	I2C1_SDA	SPI1_SOUT	eTMR1_FLT2			SPI0_SIN	SPI7_SOUT	LINFlexD7_RX			MPWM1_CH11	
		167	PTE_26		PTE_26	eTMR3_CH6	eTMR4_CH6											MPWM1_CH12	
95	139	168	PTC_5		PTC_5	eTMR2_CH0	RTC_CLKOUT	SPI3_PCS1	I2C3_SDA	eTMR2_QD_PHB	SAI0_MCLK			SPI7_SCK				MPWM1_CH13	JTAG_TDI
96	140	169	PTC_4	ACMP0_IN2/ ACMP1_IN3	PTC_4	eTMR1_CH0	RTC_CLKOUT		I2C3_SCL	eTMR1_QD_PHB									JTAG_TCK SWD_CLK
97	141	170	PTA_5		PTA_5	CAN3_TX	TCLK_IN1												RESET_b
		171	VSS	VSS															
		172	VDD_HVA	VDD_HVA															
98	142	173	PTA_4		PTA_4	CAN3_RX		ACMP0_OUT						SPI7_PCS1					JTAG_TMS SWD_IO
		174	PTE_27		PTE_27	eTMR3_CH7	eTMR4_CH7							SPI7_PCS3					
99	143	175	PTA_9	ADC0_S31	PTA_9	LINFlexD2_TX	SPI2_PCS0	SPI1_SIN	eTMR3_FLT2	eTMR1_FLT3	eTMR4_FLT0		SPI3_PCS0	SPI7_PCS2		FMU_ERR_IN2		MPWM1_CH14	

Table 31 continued from previous page

100 LQFP	144 LQFP	176 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
100	144	176	PTA_8	ADC0_S26	PTA_8	LINFlexD2_RX	SPI2_SOUT	SPI1_SCK	eTMR3_FLT3	eTMR4_FLT1			eTMR4_CH4			FMU_ERR_IN3		MPWM1_CH15	

1. ACMP0 and ACMP1 share ACMP_IN1.
2. ACMP0 and ACMP1 share ACMP_IN0.

7.2 Packages

The information of package pinouts is as follows:

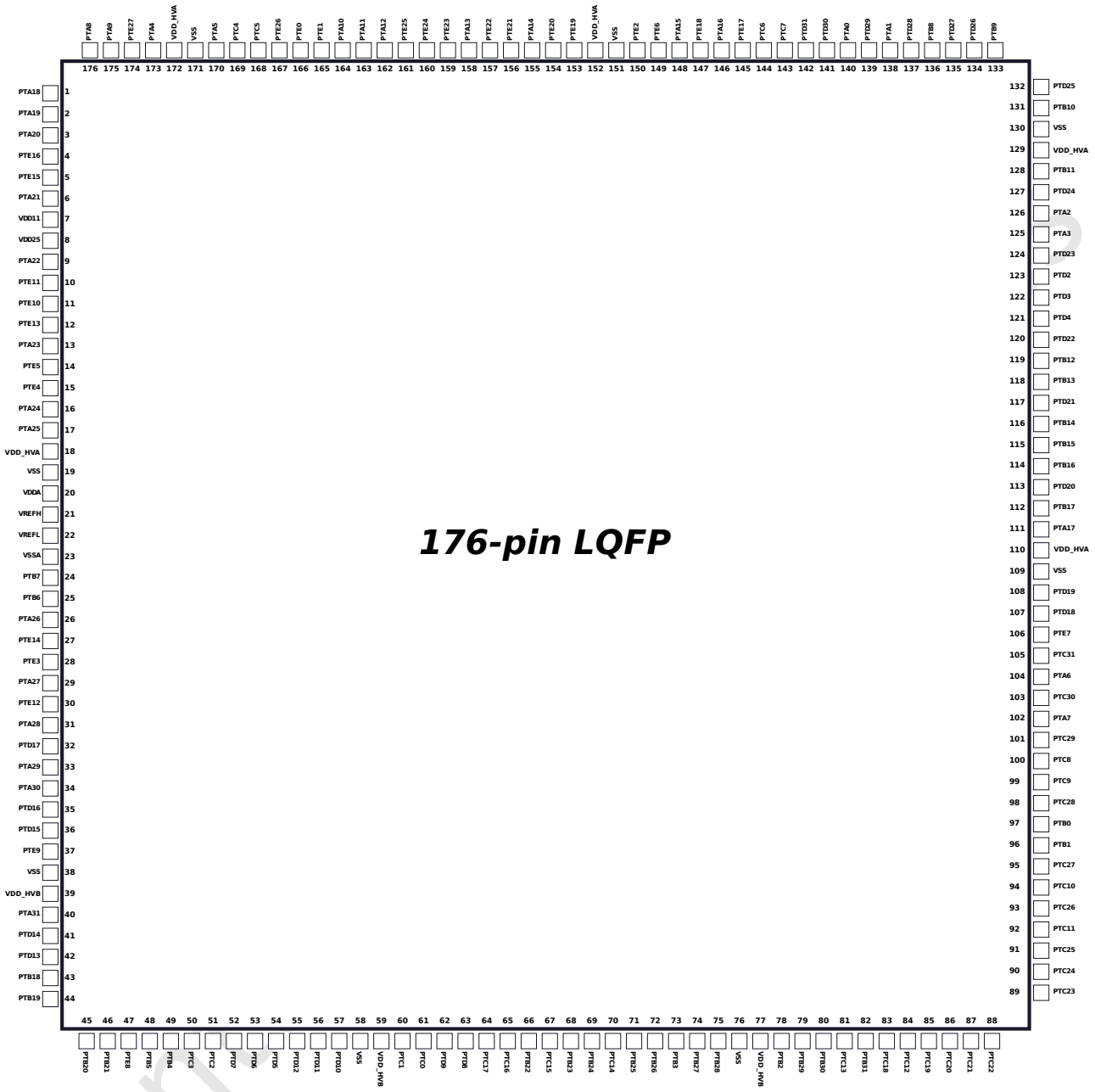


Figure 15: 176-pin LQFP Package

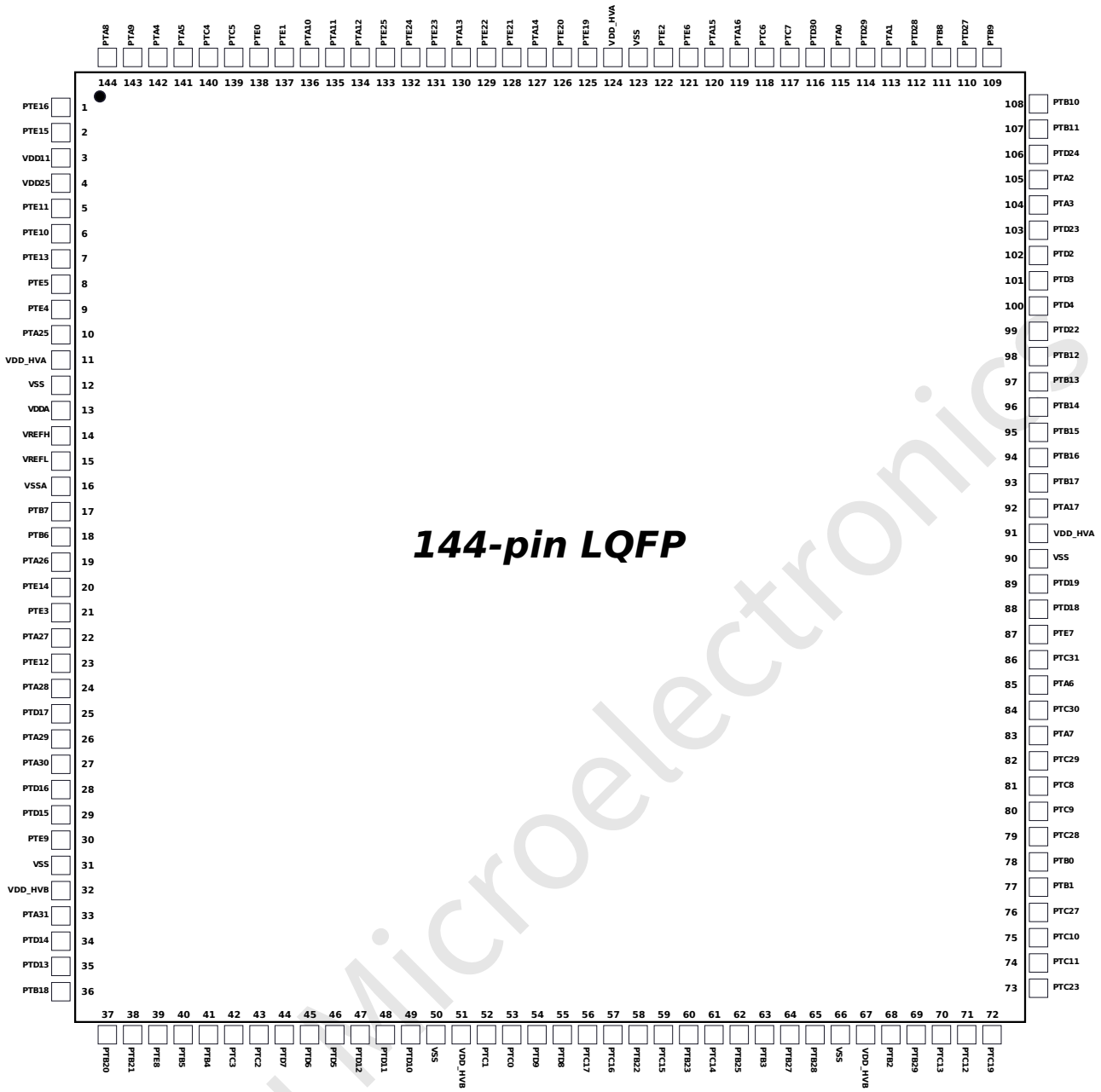


Figure 16: 144-pin LQFP Package

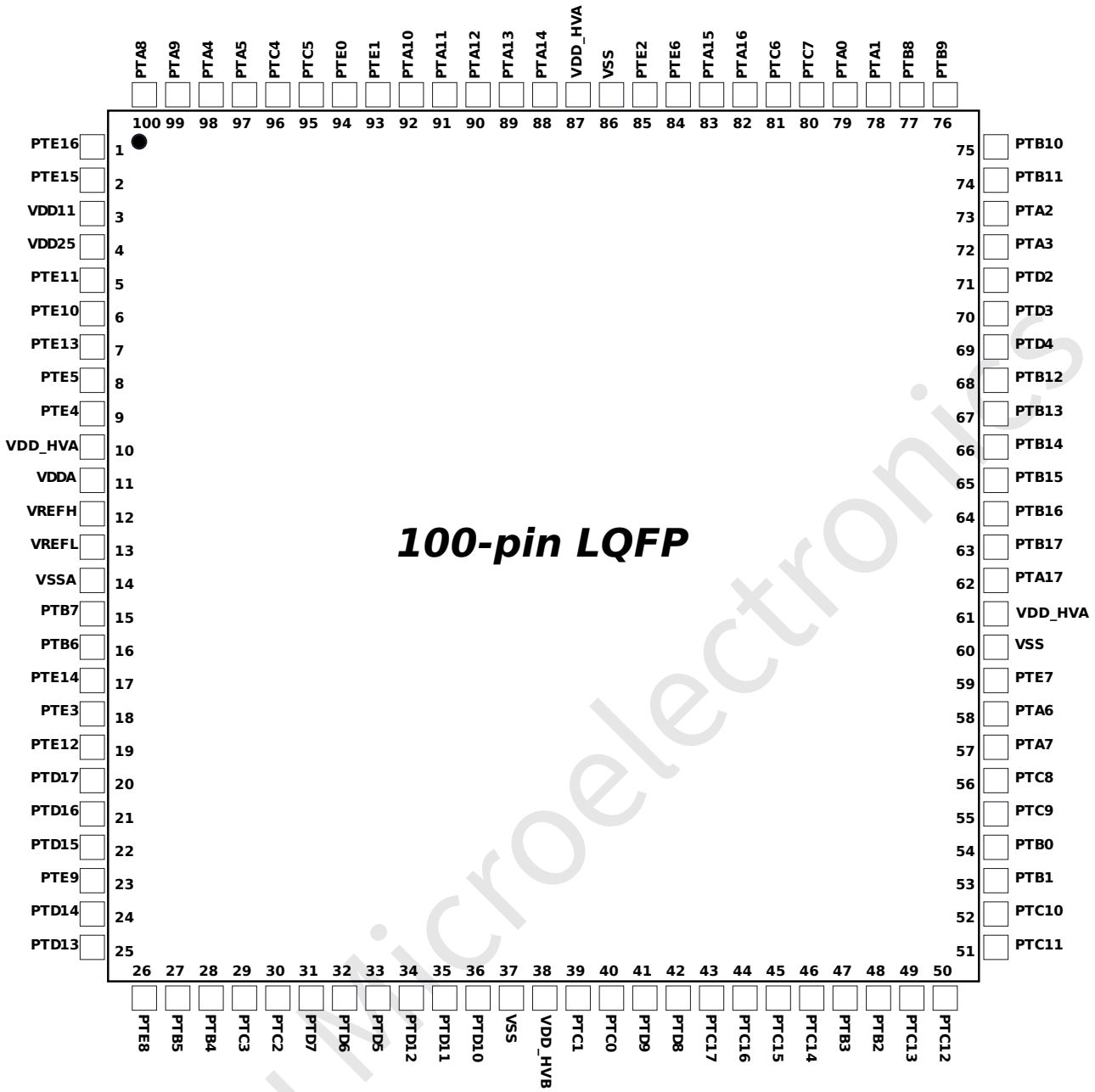
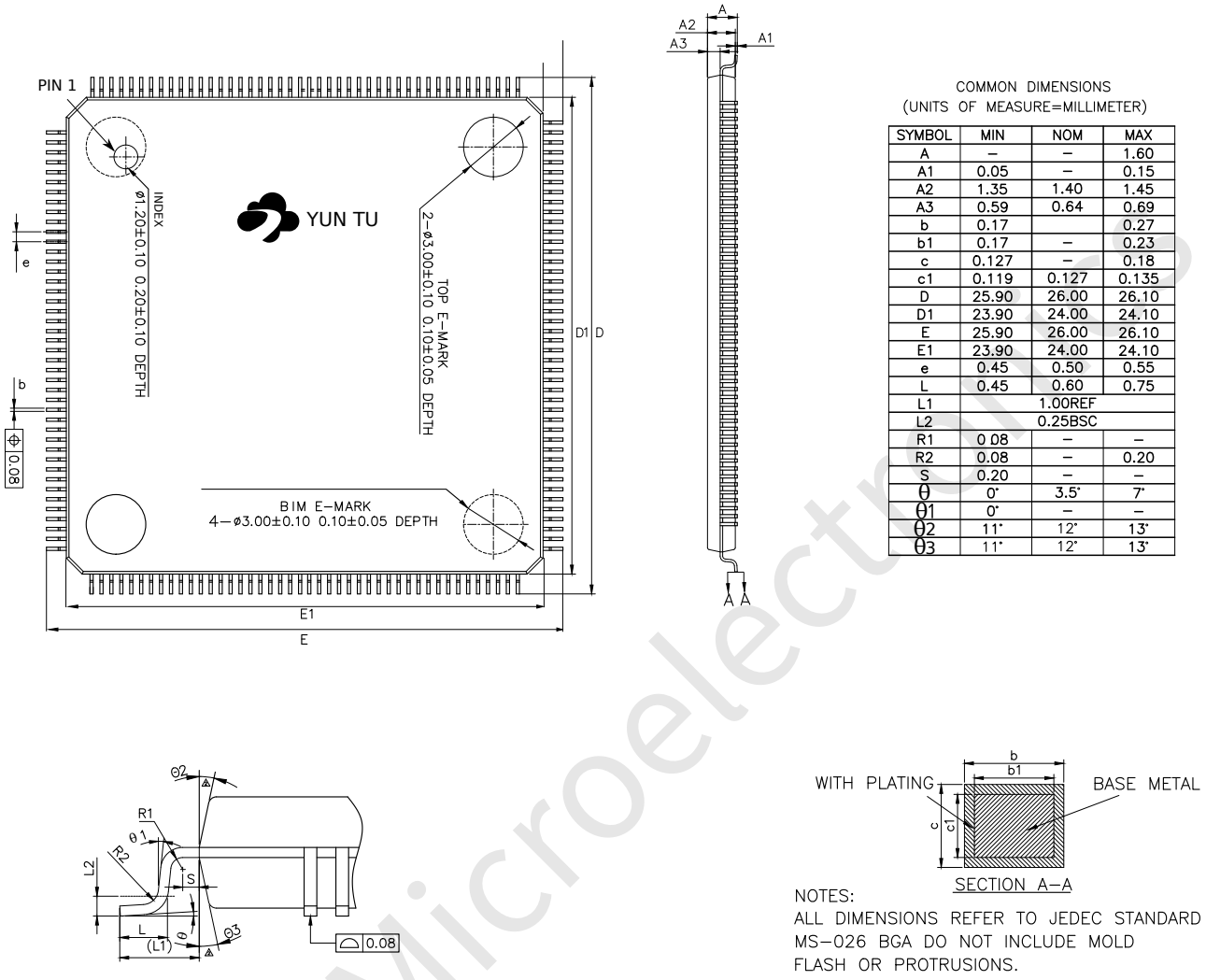


Figure 17: 100-pin LQFP Package

NOTE: The chip mark will not contain packing information(T/R)

7.3 Dimensions

Package dimensions are as follows:

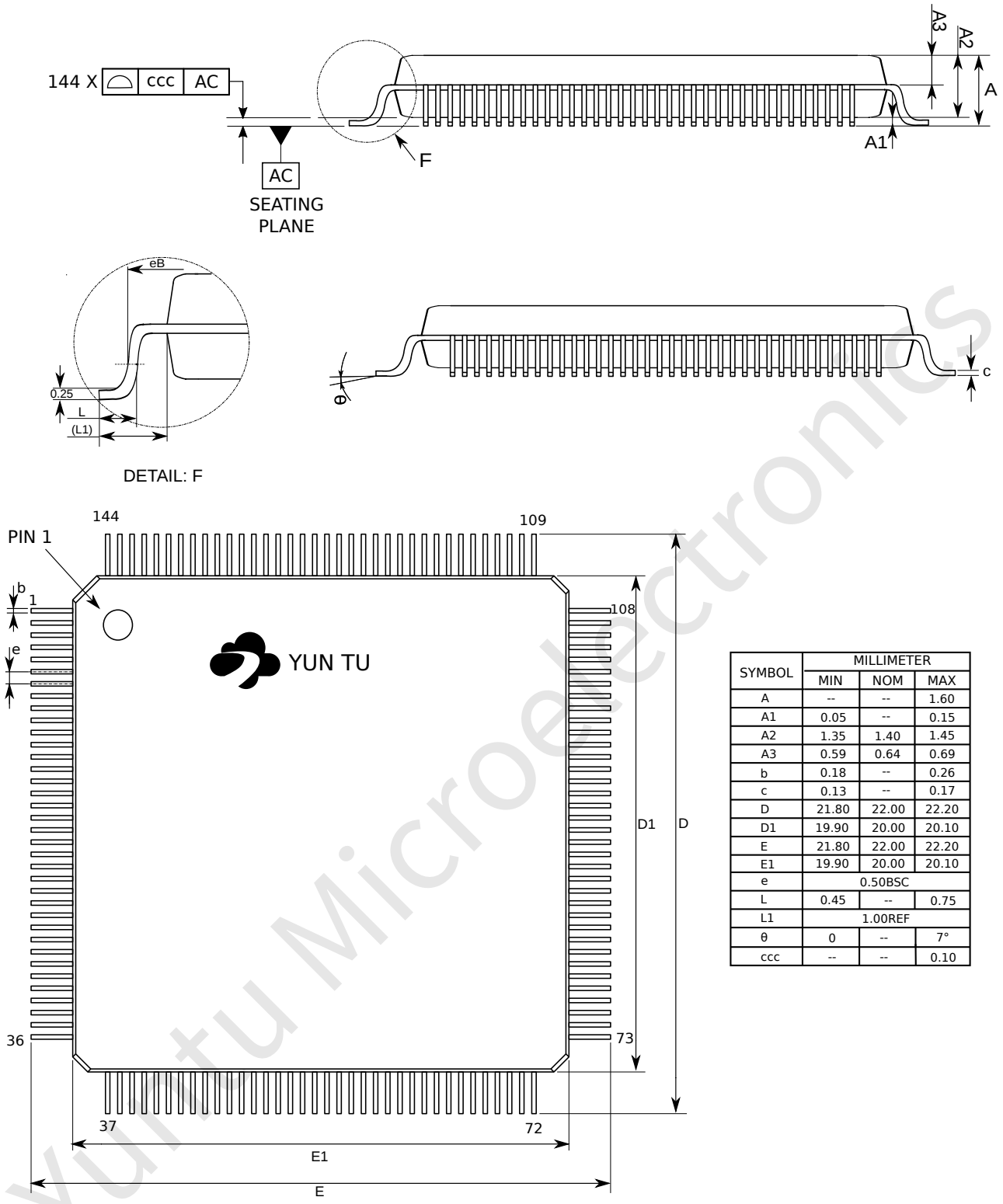


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17		0.27
b1	0.17	–	0.23
c	0.127	–	0.18
c1	0.119	0.127	0.135
D	25.90	26.00	26.10
D1	23.90	24.00	24.10
E	25.90	26.00	26.10
E1	23.90	24.00	24.10
e	0.45	0.50	0.55
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

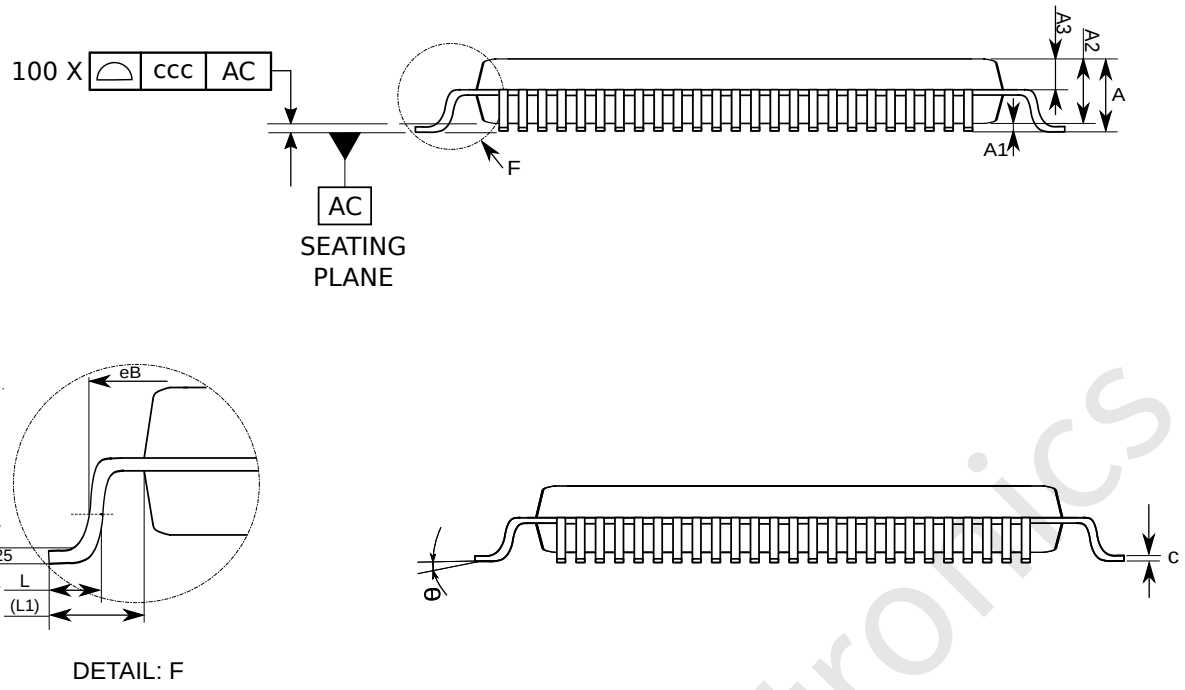
NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS–026 BGA DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

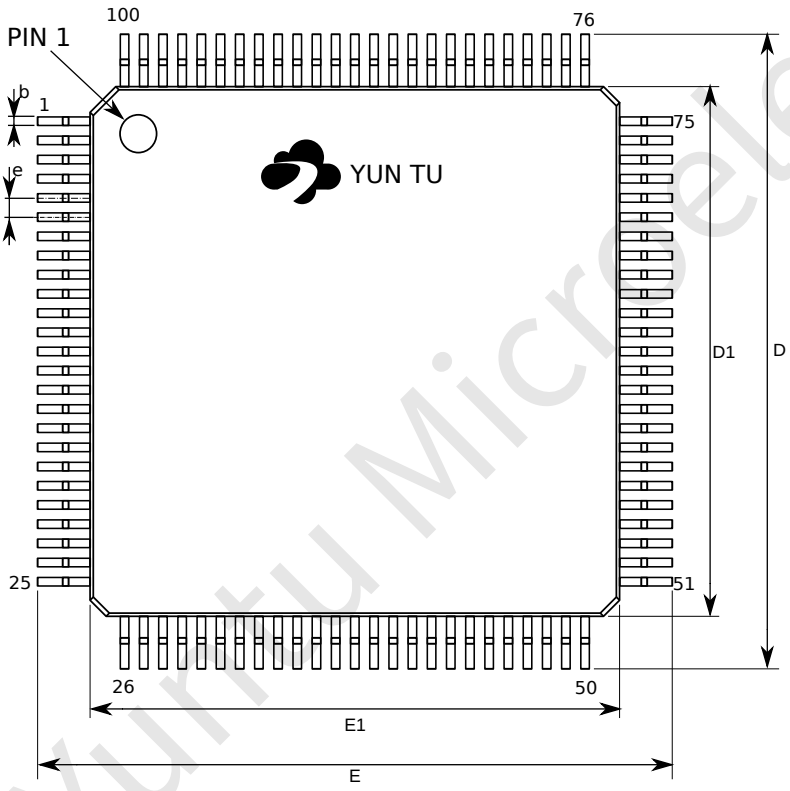
Figure 18: 176-pin LQFP



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
c	0.13	--	0.17
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°
ccc	--	--	0.10

Figure 19: 144-pin LQFP





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
c	0.13	--	0.17
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
eB	15.05	--	15.35
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°
ccc	--	--	0.08

Figure 20: 100-pin LQFP

Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2023/02/10	Initial version
1.1	2023/03/13	Added “AEC-Q100 qualified” in Features Summary Added the new section of Thermal Attributes
1.2	2023/7/31	Added “ASIL-D compliant” in Features Summary Updated the features in the subsection of Read-Only Memory(ROM) Corrected the symbol in Thermal Operating Characteristics Updated the heading of 6.2.5 to “Power and Ground Pins” Updated the table and the figure of ADC Circuit in the subsection of ADC Characteristics Updated the contents in the section of Thermal Attributes Corrected the contents in the column of ALT0 in Pinmux Table Added the coplanarity specifications of 100-pin and 144-pin LQFP in the section of Dimensions Added the location information of PIN 1 of 100-pin and 144-pin LQFP in the section of Dimensions
1.3	2023/11/1	Updated “crc” to “pcrc” in Features Summary, Block Diagram and the heading of 4.6.1 Removed some features of Analog-to-Digital Converter Updated the features of Enhanced Timer Updated the features of Hardware Cryptography Unit Added the data in ESD Handling Ratings Added the Max. value of I_{VDD} in Absolute Maximum Ratings Updated the contents of table in DC Electrical Specifications at 3.3V Updated the contents of table in DC Electrical Specifications at 5.0V Updated the figure and table in Power and Ground Pins Updated the contents of table in Power Mode Transition Operating Behaviors Updated the contents of table in Power Consumption Added the TBD data in FXOSC(4 40 MHz) Characteristics Added the TBD data in SXOSC(32.768 KHz) Characteristics Added the TBD data in FIRC(96 MHz) Characteristics Added the TBD data in SIRC(12 MHz) Characteristics Added the TBD data in ADC Characteristics Added the TBD data in ACMP Characteristics Added the TBD data in Reliability Specifications Updated the figure of “176-pin LQFP” in Dimensions

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