YTM32B1HA1x Data Sheet

Support: YTM32B1HA11S0MLUT, YTM32B1HA11S0MLQT, YTM32B1HA11S0MLLT,
YTM32B1HA10S0MLUT, YTM32B1HA10S0MLQT, YTM32B1HA10S0MLLT

Document Number: YTM32B1HA1x DS

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1 Features Summary

- AEC-Q100 qualified
- ASIL-B compliant
- RoHS compliant
- Cortex-M7 with FPU and DSP, up to 160MHz
- Debug functionality
  - Joint Test Action Group (IEEE 1149.1 standard)
  - Serial Wire Debug (SWD)
- Memories
  - Support 8KB I-Cache and 8KB D-Cache
  - Support 64KB DTCM
  - Up to 1M*2 Program Flash
    - Support ECC feature
    - Support OTA
    - Wide operating voltage range(2.97 ~ 5.5V) with fully functional Flash memory program/erase/read operations
  - Up to 192KB SRAM
    - Support ECC feature
  - 32KB retention RAM in Powerdown mode
  - 32KB on-chip ROM supports secure boot
  - 32 bytes register file
- Provide multiple clock sources including:
  - 48MHz Fast Internal RC Oscillator (FIRC)
  - 2MHz Slow Internal RC Oscillator (SIRC)
  - 4 ~ 40MHz Fast Crystal Oscillator (FXOSC)
  - 32KHz Slow Crystal Oscillator (SXOSC)
  - 160MHz Phase-Locked Loop (PLL)
- Power Control Unit (PCU) with internal regulators capable of supporting multiple power modes including:
  - Active
  - Sleep
  - Deepsleep
  - Standby
  - Powerdown
- 16 DMA channels with up to 81 hardware trigger sources
- Analog modules providing precision mixed-signal capabilities, including:
  - 2 12-bit, 2Msps SAR ADC, up to 32 external input channels, 4 internal channels and 1 external expanded channel
  - 1 On-chip Analog Comparator (ACMP) with 8-bit DAC, up to 8 channels
  - Temperature sensor
- Timers
  - 1 Timer (TMR)
  - 2 four-channel Periodic Timer (pTMR)
  - 1 Low Power Timer (lpTMR)
  - 4 eight-channel Enhanced Timer (eTMR)
  - 2 sixteen-channel Multiple Pulse Width Modulation (MPWM)
  - 1 Real-Time Clock (RTC)
- Serial communication interfaces
  - 6 FlexCAN modules with FD
  - 8 UART modules
  - 6 SPI modules
  - 3 I2C modules
  - 1 two-channel Single Edge Nibble Transmission (SENT)
- Security
  - Hardware Security Module (HSM)
    - Support AES, SM4, SHA, and HMAC
    - Support RSA, max key size 4096 bit
    - Support ECC-192, ECC-256, ECC-384
    - Support True Random Number Generator (TRNG)
    - Up to 128KB DFlash for HSM firmware and EEPROM emulation
      - Support ECC feature
- Safety features are supported as follows
  - Programmable Cyclic Redundancy Checker (PCRC)
  - Interrupt Monitor (INTM)
  - Peripheral Protection Unit (PPU)
  - Watchdog (WDG)
  - External watchdog (EWDG)
  - ECC Management Unit (EMU)
  - Low Voltage Warning (LVW), Low Voltage Detect (LVD), High Voltage Detect (HVD)
  - IO Output feedback Compare (IOOC)
  - Clock Monitor Unit (CMU)
- Human-machine interfaces
  - Up to 154 General-Purpose Input/Output (GPIO)
  - External interrupt
- I/O supporting 2.97 ~ 5.5V supply
- Temperature range:
  - Ambient operating temperature: -40 °C ~ 125 °C
  - Junction operating temperature: -40 °C ~ 150 °C
- Package options
  - 176-pin LQFP
  - 144-pin LQFP
  - 100-pin LQFP

Contents

2 Overview

The YTM32B1Hx is a family of microcontrollers built on the latest ARM® Cortex®-M7 , it offers a broad range of memory, peripherals and package options.

The YTM32B1Hx family introduces new features and uses high performance, high reliability CMOS technology to provide substantial cost reduction and significant performance improvement.

YTM32B1HA1x series of devices are 32-bit general purpose automotive microcontrollers based on the ARM Cortex-M7 core . They offer superior performance, large memories and the most scalable peripherals in this class. This product series provide up to 160MHz CPU performance, with up to 2MB PFlash, 128KB DFlash, 32KB ROM, and 256KB SRAM .

3 Block Diagram

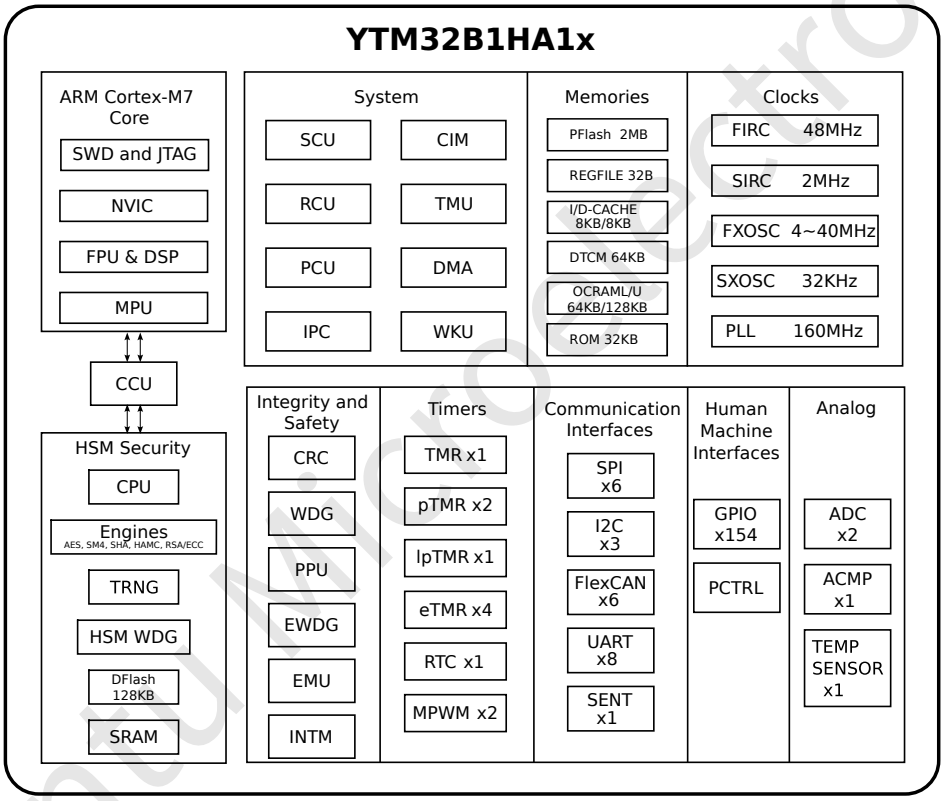


Figure 1: YTM32B1HA1x Block Diagram

4 Features

The following sections describe the high-level module features for YTM32B1HA1x device.

4.1 Core Modules

4.1.1 ARM Cortex-M7

- An in-order issue, super-scalar pipeline with dynamic branch prediction

- DSP extensions
- The ARMv7-M Thumb instruction set, defined in the Arm v7-M Architecture Reference Manual
- Banked Stack Pointer (SP)
- Hardware integer divide instructions, SDIV and UDIV
- Handler and Thread modes
- Automatic processor state saving and restoration for low-latency Interrupt Service Routine (ISR) entry and exit
- Support for ARMv7-M unaligned accesses
- Low-latency interrupt processing
- A low-cost debug solution with CoreSight components
  - Support breakpoints
  - Support watchpoints, tracing, and system profiling
  - Support printf() style debugging through an Instrumentation Trace Macrocell (ITM)
  - Support Trace Port Interface Unit (TPIU)
  - Support Debug Access Port (DAP)
- Support ETM (Embedded Trace Macrocell)
- Support Floating Point Unit(FPU)
- Support WIC
- Support memory interfaces that include
  - Harvard architecture-based instruction and data caches, and an AXIM interface
  - A dedicated low-latency AHBP interface
  - A 64-bit AXI AMBA4 memory interface with a 8 KB instruction cache and an 8 KB data cache for efficient access to external resources. The instruction and data caches are ECC protected.
  - A 32-bit AHBS for interfacing with slaves
  - 64-bit and 32-bit memory interfaces for the connection to local Tightly Coupled Memories called ITCM and DTCM
  - Cortex-M7 core interfaces with low-latency 32 KB DTCM0 and 32KB DTCM1
  - Support 16 regions MPU

4.1.2 Nested Vector Interrupt Controller (NVIC)

- Up to 240 interrupt sources
- Support 16 priority levels for interrupts with three bits in each IPRn registers
- Include a single non-maskable interrupt

4.1.3 Debug Controller

- 2-pin Serial Wire Debug (SWD) provides external debugger interface
- Support JTAG port (IEEE 1149.1 standard)

4.2 System Modules

4.2.1 System Clock Unit (SCU)

- Fast internal RC oscillator(FIRC)
  - Up to 48 MHz
  - Default system boot clock source
  - Support trim for temperature and process
  - Can be selected as PLL reference clock
- Slow Internal RC Oscillator(SIRC)

  - 2 MHz
  - Can be selected as system clock source
  - Always on unless it is forced to be disable in standby mode
  - Support trim for temperature and process
- Fast Crystal Oscillator(FXOSC)
  - Support 4~40MHz crystal
  - Can be selected as PLL reference clock
  - Can be selected as system clock source
  - Support bypass mode
- Slow crystal oscillator(SXOSC)
  - 32.768 KHz real time oscillator
  - Can't be selected as system clock
  - Provides accurate clock to watchdog(WDG) and real time clock(RTC)
- Phase-Locked Loop(PLL)
  - Up to 160 MHz
  - Contains Voltage-controlled Oscillator(VCO)
  - Support selectable reference clock
  - Contain Frequency lock detector
  - Can be selected as system clock source
- Clock Monitor Unit(CMU)
  - SCU contains 4 CMU blocks
  - CMU monitors slow bus clock, FIRC clock, FXOSC clock and PLL clock
  - FXOSC or SIRC clock can be selected as reference clock of CMU
  - CMU can detect frequency out of range, loss of checked clock and loss of reference clock
- SCU provides glitch free switcher to select system clock source
- SCU provides system clock dividers to generate fast bus clock, slow bus clock and core clock

4.2.2 Power Control Unit (PCU)

- Combination of internal and external voltage regulator options, offering a variety of power modes
- Active POR providing brown-out detect
- Low voltage detect(LVD) reset for all system relevant power domains
- Low voltage warning(LVW) as indication for software or as an interrupt source
- High voltage detect (HVD) as indication for software or as an interrupt source or as a reset source.

4.2.3 Reset Controller Unit (RCU)

- Record the reset sources of most recent resets.
- Configurable filter for reset pin.
- Reset pin filter can work in Active, Sleep, Deepsleep Standby mode.
- Reset monitor counter to the record the reset events

4.2.4 IP Controller (IPC)

- Peripheral Bus clock enable
- IPC clock source selection from multiple clock sources
- IPC clock divide values from 1 to 16
- Peripheral software reset

4.2.5 Direct Memory Access (DMA)

- All address range data transfer from source to destination
- Support separate source/destination data size configuration
- Word(32-bit), half word(16-bit), byte(8-bit) transfer size
- Support separate source/destination address offset configuration
- Address increase/decrease/keep selectable
- Up to 16 DMA channels
- Fix priority and round-robin arbitration
- Support channel to channel link
- Software/Hardware/Link trigger
- Up to 81 peripheral hardware triggers
- Internal data FIFO for data transfer
- Support update DMA transfer information from system memory after transfer complete
- Support data transfer loop and trigger loop

4.2.6 Trigger Multiplex Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources

4.2.7 Chip Integration Module (CIM)

- System function configuration
- ADC and ACMP trigger synchronize selection
- Software trigger generate
- eTMR external clock, fault and channel input selection
- eTMR output modulation configuration
- FPU interrupt enable
- Flash memory and system RAM size configuration
- Package configuration
- FlexCAN FD feature configuration
- System boot configuration

4.2.8 Wake-up Unit (WKU)

- Support for up to 32 external input pins and up to 3 internal modules with individual enable bits for MCU interrupt from Powerdown mode.
- Input sources may be external pins or from internal modules capable of running in Powerdown mode.
- External input pins programmable for falling-edge, rising-edge, or any-edge detection.
- Support to enable external input pin and filter detection in Powerdown mode.
- Optional digital filters provided to qualify an external pin detect. Note that when the SIRC and SXOSC clock is disabled, filters are disabled and bypassed.

4.3 Memories

4.3.1 Embedded Flash Module (EFM)

- Program Flash (PFlash) support 2MB address space
  - PFlash support ECC 1-bit error correction and 2-bit error detetion (SEC-DED)
  - Support read-while-write and OTA (Over-The-Air) technology

- Protection scheme against accidental program or erase operations
- Command protection function for authorization protection
- Optional interruptions on command completion and status update
- Support prefetch read to improve AHB read performace
- Support read buffer to improve AHB read performace

4.3.2 On-Chip RAM (OCRAM)

- Up to 192KB
- Support 32/16/8bit access
- Support ECC safety function
  - 64bit data and 8bit ECC code
  - Single bit error correction
  - Double bit error detection
- Support RAM retention in Powerdown mode

4.3.3 Read-Only Memory (ROM)

- ROM boot firmware is programmed by YTMicro to support secure boot, fast wake-up from Powerdown Mode, and System clock configuration
  - Run once the chip releases the reset signal of the CM7 core
  - Support BVT parse and execute the enabled functions per configuration
  - Configured according to user configuration via BVT (Boot Vector Table)
- Secure boot
  - Work as the root of trust
  - Support CMAC/HMAC authorization (by using HSM) of customized code (for example, the bootloader/OTA) with specified start address and length via secure boot group and section configuration structure (support up to 8 secure boot sections)
  - The used HSM hardware user keys for secure boot section configuration structure encryption and CMAC/HMAC authorization should be pre-programmed to HSM_NVR memory by the Car OEM or Tier-1 using the flash programmer
- Support strict serial secure boot mode (enabled via BCW of BVT)
  - If CMAC/HMAC authorization fails, the secure boot holds the CM7 core in static mode
- Support normal secure boot mode (by default)
  - If CMAC/HMAC authorization fails, the CM7 core continues to execute the bootloader and the applications, but all HSM hardware keys will be disabled or fail to load.
- Fast wake-up from Powerdown Mode
  - Support fast wakeup after resetting from Powerdown mode
  - Reduce the ROM boot time by ignoring secure boot and core test
  - Enable and configuration of the needed separated application IVT (Interrupt Vector Table) are achieved by the CIM software define registers (which are retained during Powerdown mode)
- System clock configuration
  - Support enables PLL in RomBoot to speed up startup stage.
- HSM FW verify and install
  - Supports HSM validation and startup during the boot phase. Once the HSM is installed, both the CM7 core and the Data-Flash are managed by the HSM.
  - More detail see HSM RM.

4.3.4 Register File (REGFILE)

- 32 bytes register file to retain value during Powerdown mode.

- Access through APB bus.

4.4 Analog

4.4.1 Analog-to-Digital Converter (ADC)

- Contain 2 ADC instances
  - ADC0 supports up to 32 external analog input channels, and 4 internal channels and channel expansion
  - ADC1 supports up to 32 external analog input channels, and 4 internal channels and channel expansion
- Support 12-bit, 10-bit, 8-bit and 6-bit single-ended configurable resolution
- Up to 2 Msps for 12-bit resolution conversion performance
- Support DMA and conversion result FIFO with watermark
- Support multiple conversion modes
  - Single mode
  - Continuous mode
  - Discontinuous mode
- Support software/hardware trigger for ADC start conversion
- Support two power saving modes
  - Wait mode: prevent ADC overrun when FIFO is full
  - Auto off mode: automatic control ADC power off
- Support watchdog for conversion result monitoring
- Support inject sequence conversion
- Support interrupt generate
  - Ready for conversion
  - End of sampling
  - End of conversion
  - End of sequence conversion
  - Overrun event
  - Watchdog event
  - Inject conversion event
  - Normal trigger source lose error event
  - Inject trigger source lose error event
- Support work and wake up when the chip is under sleep and deepsleep modes

4.4.2 Analog Comparator (ACMP)

- Up to 8 channels
- Operational over the entire supply range
- ACMP DAC Buffer inputs may range from rail to rail
- Programmable hysteresis control
- Selectable inversion on comparator output
- Function mode:

  - Common mode
  - Sample mode
  - Window mode
  - Continuous mode
    - One-shot mode
    - Loop mode
- All channels can be used to execute automatic comparison
- Support digital filter, the filter can be bypassed
- Two software selectable performance levels
  - Shorter propagation delay at the expense of higher power
  - Low power with longer propagation delay
- Functional in all power mode
- Support independent 8-bit DAC output to the comparator
- Support several interrupts
  - For common/sample/window mode
    - Generate interrupt on rising-edge, falling-edge or both edges of the comparator output or generate interrupt when comparator output is high or low
  - For continuous mode
    - Generate interrupt when the comparison results don't match with expectations
- Interrupt can be generated without any clock in common mode
- A comparison event can be selected to trigger DMA transfer

4.5 Timer

4.5.1 Timer (TMR)

- One 32-bit count-up timer with an 8-bit prescaler
- Four 32-bit compare channels
- An independent interrupt source for each channel
- Ability to stop the timer in debug mode

4.5.2 Periodic Timer (pTMR)

- Timers can generate interrupts, and each channel can generate independent interrupt request
- Four channels of 32-bit timers, each timer has independent timeout periods
- Ability to stop in debug mode
- Support chain mode to connect multiple timer to a longer timer

4.5.3 Low Power Timer (lpTMR)

The features of the lpTMR module include:

- 16-bit time counter or pulse counter with compare
- Optional interrupt can generate asynchronous wakeup from any Low-power mode
- Hardware trigger output
- Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

4.5.4 Enhanced Timer (eTMR)

The common features contained in all eTMRs are listed below:

- Configurable initial and final counter values
- Contain 8 channels
- Support two clock sources
  - Bus clock
  - External clock
- Support 7-bits clock prescaler
- Support four channel modes
  - Common timer
  - PWM mode
    - Independent mode for each channel
    - Complementary mode for each pair of channels
      - Odd channels and even channels support independent deadtime insertion
    - Support dithering
    - Channel output control (initialization, software control, mask control, double switch control, fault control)
      - Support 4 fault input sources
      - Support fault input from TMU or pad
      - Support fault input polarity control
      - Support fault input filter
      - Support fault input stretch
      - Support fault event generated by combinational logic
    - Relevant registers have buffer registers and support loading mechanism
  - Output Compare mode
    - The output can be configured to set, clear or toggle on match point
  - Input Capture mode
    - Support rising edges, falling edges or dual edges capture
    - Support input filter with a prescaler
    - Support capture test mode
    - Support pulse width measure
- Support generating triggers
  - Output triggers with adjustable pulse width on match point
  - Output pulse with adjustable width by PWM
- Polarity control is available for each channel
- Support GTB (Global Time Base)
- Support several interrupts
  - Channel interrupt (capture interrupt and compare interrupt)
  - Counter overflow interrupt
  - Fault event interrupt
- Support DMA
- Support counter running under debug mode

- Supports hall sensor input
- Support input from ACMP

4.5.5 Multiple Pulse Width Modulation (MPWM)

- Each MPWM supports 16 channels
- Each channel contains a 16-bit counter independently
  - Configurable comparison value
  - Configurable period value
- Support clock prescaler(1, 2, 4, 8, 16, 32, 64, 128) independently
- Counting modes
  - Continuous mode
  - One shot mode
- Support counter starts counting by hardware trigger in one shot mode
- Support four channel modes
  - Common timer
  - PWM mode
    - Independent mode for each channel
    - Support edge-aligned PWM
    - Relevant registers have double buffer registers and support loading mechanism
    - Write operations to double buffer registers take effect immediately
  - Output Compare mode
    - The output can be configured to set, clear or toggle on match point
  - Input Capture mode
    - Support rising edge capture
    - Support falling edge capture
    - Support any edge capture
    - Support combination capture
  - Pulse count mode
- Support generating triggers on match point
- Polarity control is available for each channel
- Support several interrupts
  - Channel event interrupt
  - Timer overflow event interrupt
- Support DMA
- Support hall sensor input
- Support input from ACMP
- Support counter running under debug mode

4.5.6 Real Time Clock (RTC)

- Register write protection for RTC enable register
- 32-bit seconds counter with overflow flag, second flag and their optional interrupt
- 32-bit alarm register, support report alarm flag and optional interrupt
- Configurable 1, 2, 4, 8, 16, 32, 64 or 128 Hz square wave output with optional interrupt
- 16-bit prescaler with compensation that can correct second errors and configure compensation interval
- Software reset for all register
- Support enter debug mode
- Support select clock source for counter, and support select output clock source

4.6 Security, Integrity and Safety

4.6.1 Programmable Cyclic Redundancy Check (PCRC)

- Programmable CRC polynomials
- Programmable initial seed
- Optional bit-swap in one byte is available for input and output data
- Optional bit-swap in one word is available for input and output data
- Optional byte-swap in one word is available for input and output data
- Optional bit-inversion is available for output data
- 8/16/32-bit access for CRC input data

4.6.2 Hardware Security Module (HSM)

- All crypto-related features are accelerated by our hardware crypto engine
- Powerful cross-core IPC hardware peripherial (CCU)
- Flexible key management, key partition, support three types of keys:
  - ROOT KEY
  - NVR KEY
  - RAM KEY
    The size of Max keys depends on the format of key partitions.
- Security related features:
  - AES, includes CCM, max key size 256 bit
  - HMAC/CMAC, max key size 256 bit
  - RSA, max key size 4096 bit
  - ECC-192, ECC-256, ECC-384
  - SM4, max key size 128 bit
  - SM2
  - SHA2-256, SHA2-384
  - TRNG
- FEE integrated features. HSM FW manages all data flash regions, so HSM contains FEE init-, write-, read- and invalid-related features
- Data Flash (DFlash) supports 128KB address space
  - DFlash supports ECC 1-bit error correction and 2-bit error detetion (SEC-DED)

4.6.3 ECC Management Unit (EMU)

- 5 channels of ECC injection and report
- Two-stage enable mechanism for ECC injection
- Location and correctable or uncorrectable error can be injected
- ECC error interrupt can be enabled with separated register bit
- The last ECC error data can be recorded into register

4.6.4 Interrupt Monitor (INTM)

- Up to 8 programmable monitors
- Programmable monitored interrupt source per monitor
- Programmable 24-bit latency counter per monitor
- Programmable 24-bit counter threshold per monitor
- Timer expired status bit per monitor

- One overall interrupt acknowledge for all monitors
- One overall enable for all monitors
- Support injection test mode

4.6.5 Peripheral Protection Unit (PPU)

- Write access for the module under protection can be restricted to the supervisor mode only
- Multiple ways are present to set the lock bits
- Once the lock bits are set, the registers could be protected from modification

4.6.6 Watchdog (WDG)

- 32-bit countdown timer
- Functional clock can be selected from multiple clock sources
- Support regular or window servicing mode
- Support reset request or interrupt for the first timeout
- Hard and soft configuration lock bits

4.6.7 External Watchdog (EWDG)

- Independent functional clock source
- Programmable time-out period
- Windowed refresh option
- Provides robust check that program flow is faster than expected
- Programmable window
- Refresh operation should be done within 63 peripheral bus clock cycles
- An output pad EWDG_OUT_b is used to indicate operation error
- An input pad EWDG_IN is used for external circuit to control EWDG_OUT_b output directly

4.7 Communication Interfaces

4.7.1 Flexible Controller Area Network (FlexCAN)

- Full implementation of the CAN FD protocol and CAN Specification 2.0, Part B
  - Standard data frames
  - Extended data frames
  - Zero to sixty-four bytes data length
  - Programmable bit rate
  - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Silicon-proven implementation passing ISO 16845-1:2016 CAN conformance tests
- Flexible mailboxes configurable to store 0 to 8, 16, 32, or 64 bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Legacy Rx FIFO with storage capacity for up to 6 CAN frames and automatic internal pointer handling with DMA support
- Full-featured Enhanced Rx FIFO with storage capacity for up to 32 CAN FD frames and automatic internal pointer handling with DMA support
- Transmission abort capability

- Flexible message buffers, totaling 128 message buffers of 8 bytes data length each, configurable as Rx or Tx
- Programmable clock source to the CAN Protocol Engine, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer, with an optional external time tick or high-resolution 32-bit on-chip timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the FlexCAN is synchronous with CAN bus
- CRC status for transmitted message
- Legacy Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Legacy Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 ID Filter Table elements
- Powerful Enhanced Rx FIFO ID filtering, capable of matching incoming IDs against either 64 extended or 128 standard ID filter elements with three filtering schemes: mask + filter, range, and two filters without mask
- 100% backward compatibility with previous FlexCAN version
- Support in low power modes: Deepsleep mode and Standby mode

4.7.2 Universal Asynchronous Receiver/Transmitter (UART)

- Support LIN break send and detect
- Transmit/Receive FIFO
- Support Transmit/Receive via DMA
- Baudrate setting
- 1-bit or 2-bit STOP size
- 7-bit, 8-bit, 9-bit or 10-bit frame size
- Transmit/Receive polarity setting
- Receive data match
- Line idle, address match wakeup
- Support transmit/receive line switch
- Support hardware flow control (CTS/RTS)
- Support single wire mode

4.7.3 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration
- Configurable frame size
- Transmit/Receive FIFO
- Support Transmit/Receive via DMA
- Support Standard/Dual/Quad SPI mode
- Support I2S standard transfer
- Support Master and Slave mode

4.7.4 Inter-Integrated Circuit (I2C)

Features of the I2C module include:

- Support standard, fast, fast plus, high speed and ultra fast mode
- Support 7-bit/10-bit address mode with master and slave
- Support SMBus mode
- Support multi-master arbitration and synchronization
- Support master and slave clock stretching
- Transmit/Receive FIFO (master only)
- Digital filter on both SCL and SDA pins
- Support transmit/receive via DMA

4.7.5 Single Edge Nibble Transmission (SENT)

- Always acts as a receiver
- Support selectable functional clock for message receiving
- Support 2 channels for different devices
- Support SENT protocol specification J2716 JAN2010
- Support programmable input filter for each channel
- Support configurable receive tick times from 1μs to 90μs for each channel
- Support auto compensation for variation in SENT transmit clock up to $\pm$ 25%
- Support configurable number of data nibbles for each channel
- Support status nibble optionally included in the checksum
- Support pause pulse for each channel
- Support separate channel buffer for storing Fast and Slow Serial Message
- Support FIFO mode to store Fast Message from all channels (Depth 8)
- Support DMA to access Fast and Slow Serial Message
- Support time stamp for all receive message
- Support varied interrupts
  - Fast Message receive interrupt
  - Slow Serial Message receive interrupt
  - Channel receive error interrupt
  - FIFO/buffer overflow and underflow interrupt
  - Wake up interrupt (any channel busy to trigger)

4.8 Human Machine Interface

4.8.1 General Purpose Input/Output (GPIO)

Features of the GPIO module include:

- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- Inversion for data inputs
- Interrupt flag and enable registers for each pin
- Support for edge sensitive (rising, falling, both) or level sensitive (low, high)
- Asynchronous wake-up in low-power modes
- Pin interrupt is functional in all digital pin muxing modes
- Support getting state of the port in all digital pin muxing modes

4.8.2 Port Controller (PCTRL)

The PCTRL module has the following port control features:

- Individual pull control fields with pullup, pulldown, and pull-disable support
- Individual slew rate field supporting fast and slow slew rates
- Individual input passive filter field supporting enable and disable of the individual input passive filter on selected pins
- Individual drive strength field supporting low or high drive strength on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to 14 chip-specific digital functions
- Individual digital filter for data inputs
- Output Compare(readback) function enable on selected pins with digital filter
- Individual lock function to avoid misoperation

5 Ordering Information

The following chips are available for ordering.

Table 1: Ordering table

Product	Memory		Package		IO and ADC channel		Communication
Part number	Flash	SRAM	Pin count	Package	GPIO	ADC	FlexCAN
YTM32B1HA11S0MLUT	2MB	256KB	176	LQFP	154	65	6
YTM32B1HA11S0MLQT	2MB	256KB	144	LQFP	126	49	6
YTM32B1HA11S0MLLT	2MB	256KB	100	LQFP	87	33	6
YTM32B1HA10S0MLUT	1MB	256KB	176	LQFP	154	65	6
YTM32B1HA10S0MLQT	1MB	256KB	144	LQFP	126	49	6
YTM32B1HA10S0MLLT	1MB	256KB	100	LQFP	87	33	6

5.1 Part Number Information

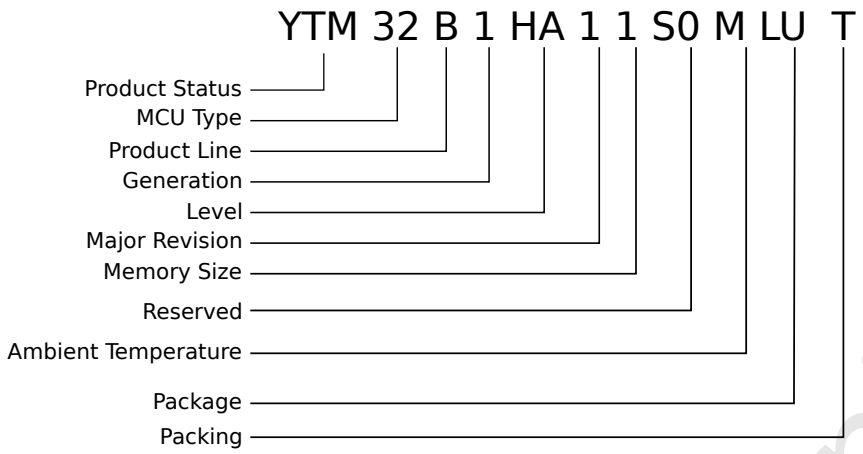


Figure 2: Part Numbers Field

Table 2: Part Number Field Description

Field	Description	Values							
YTM	Product Status	YTM: Qualified PTM: Prototype							
32	MCU Type	32: 32-bit							
B	Product Line	B: General D: Dashboard P: Powertrain V: Vision N: Network Z: High voltage, integrity							
1	Generation	1st generation production							
Hx	Level	Product Line							
		B			Hx: High end Mx: Middle end Lx: Low end				
		Z			Mx: Motor+LIN-PHY Lx: LIN-PHY Cx: CAN-PHY Tx: Touch-sensor Dx: LED Driver				
0	Major Revision	1st revision							
1	Memory Size		0	1	2	3	4	5	6
		Z	-	-	-	32K	48K	64K	128K
		H	1M	2M	4M	6M	8M	12M	16M
		M	-	-	128K	256K	512K	1M	2M
		L	-	-	-	32K	64K	128K	256K
G0	Reserved	Reserved							

Table 2 continued from previous page

Field	Description	Values					
M	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C					
LU	Package	Pins	LQFP	QFN	SOP	BGA	
		8	-	-	SB	-	-
		10	-	-	SC	-	-
		12	-	-	SD	-	-
		14	-	-	SE	-	-
		16	-	-	SF	-	-
		20	-	-	SH	-	-
		24	-	FK	-	-	-
		32	LE	FM	-	-	-
		48	LF	FN	-	-	-
		64	LH	FO	-	-	-
		100	LL	-	-	MH	-
		144	LQ	-	-	-	-
		176	LU	-	-	-	-
		208	-	-	-	MK	-
		257	-	-	-	MM	-
		289	-	-	-	MQ	-
		320	-	-	-	MR	-
		373	-	-	-	MS	-
		416	-	-	-	MT	-
		516	-	-	-	MV	-
S	Optional Mode	S: Single end mode D: Differential mode I: ISELED C: Cost Optimization X: ISELED and Cost Optimization					
T [1]	Packing	T: Trays/Tubes R: Tape and Reel					

1. The chip mark doesn't contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ M-Grade\ Part}$	Ambient temperature under bias	-40	–	125	°C

Table 3 continued from previous page

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{J\ M-Grade\ Part}$	Junction temperature under bias	-40	–	150	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	TBD	TBD	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	TBD	TBD	V	
	Corner pins only	TBD	TBD	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	TBD	TBD	mA	3
	Latch-up current at ambient temperature of 25 °C	TBD	TBD	mA	

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

6.2 DC Characteristics

6.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	-0.3	5.8[1]	V	
I_{VDD}	Maximum current into V_{DD}	–	50	mA	
V_{IO}	Digital/Analog IO Input voltage	-0.3	V_{DD} + 0.3	V	
I_O	Instantaneous maximum current of single pin	-25	25	mA	
V_{DDA}	Analog supply voltage	V_{DD} - 0.3	V_{DD} + 0.3	V	

1. 60 seconds lifetime - No restrictions i.e. the part is not held in reset and can switch.
10 hours lifetime - The part is held in reset by an external circuit i.e. the part cannot switch.

NOTE:

- The maximum ratings are the limits to which the device can be subjected without permanently damaging the device.
- The device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2.2 Voltage and Current Operating Requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.97	5.5	V	
V_{DDA}	Analog supply voltage	2.97	5.5	V	
V_{REFH}	Reference voltage	2.97	5.5	V	
$V_{DD} - V_{DDA}$	V_{DD} to V_{DDA} differential voltage	-0.1	0.1	V	
I_{ICIO}	DC injection current - single pin				
	$V_{IN} < V_{SS}$ - 0.3V (Negative current injection)	-3	–	mA	1
	$V_{IN} < V_{SS}$ + 0.3V (Positive current injection)	–	3	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of positive rejection currents of 16 contiguous pins	–	25	mA	

1. All pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{SS} – 0.3V or greater than V_{DD} + 0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{SS}–0.3V–V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R = [V_{IN}–(V_{DD} + 0.3V)]/|I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.

6.2.3 DC Electrical Specifications at 3.3V

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	2.97	3.3	4.0	V	
V_{ih}	Input buffer high voltage	0.7 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.3 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	TBD	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	–	TBD	–	mA	

Table 8 continued from previous page

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	TBD	–	mA	
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	–	TBD	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	TBD	–	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	TBD	–	nA	
V_{OH}	Output high voltage					
	Normal drive pad ($2.97V \leq V_{DD} \leq 4.0V$, I_{OH} = -2.8mA)	TBD	–	–	V	
V_{OL}	Output low voltage					
	Normal drive pad ($2.97V \leq V_{DD} \leq 4.0V$, I_{OL} = -2.8mA)	–	–	TBD	V	
I_{OLT}	Output low current total for all ports	–	–	TBD	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins @25°C	–	TBD	–	nA	
	All pins other than high drive port pins @125°C	–	TBD	–	nA	
R_{PU}	Internal pull-up resistors	TBD	–	TBD	kΩ	
R_{PD}	Internal pull-down resistors	TBD	–	TBD	kΩ	

6.2.4 DC Electrical Specifications at 5.0V

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	4	5	5.5	V	
V_{ih}	Input buffer high voltage	0.65 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.35 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	TBD	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	–	TBD	–	mA	
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	TBD	–	mA	

Table 9 continued from previous page

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	–	TBD	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin) @25°C	–	TBD	–	nA	
	Hi-Z (Off state) leakage current (per pin) @125°C	–	TBD	–	nA	
V_{OH}	Output high voltage					
	Normal drive pad ($2.97V \leq V_{DD} \leq 4.0V$, I_{OH} = -2.8mA)	TBD	–	–	V	
V_{OL}	Output low voltage					
	Normal drive pad ($2.97V \leq V_{DD} \leq 4.0V$, I_{OL} = -2.8mA)	–	–	TBD	V	
I_{OLT}	Output low current total for all ports	–	–	TBD	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins @25°C	–	TBD	–	nA	
	All pins other than high drive port pins @125°C	–	TBD	–	nA	
R_{PU}	Internal pull-up resistors	TBD	–	TBD	kΩ	
R_{PD}	Internal pull-down resistors	TBD	–	TBD	kΩ	

6.2.5 Power and Ground Pins

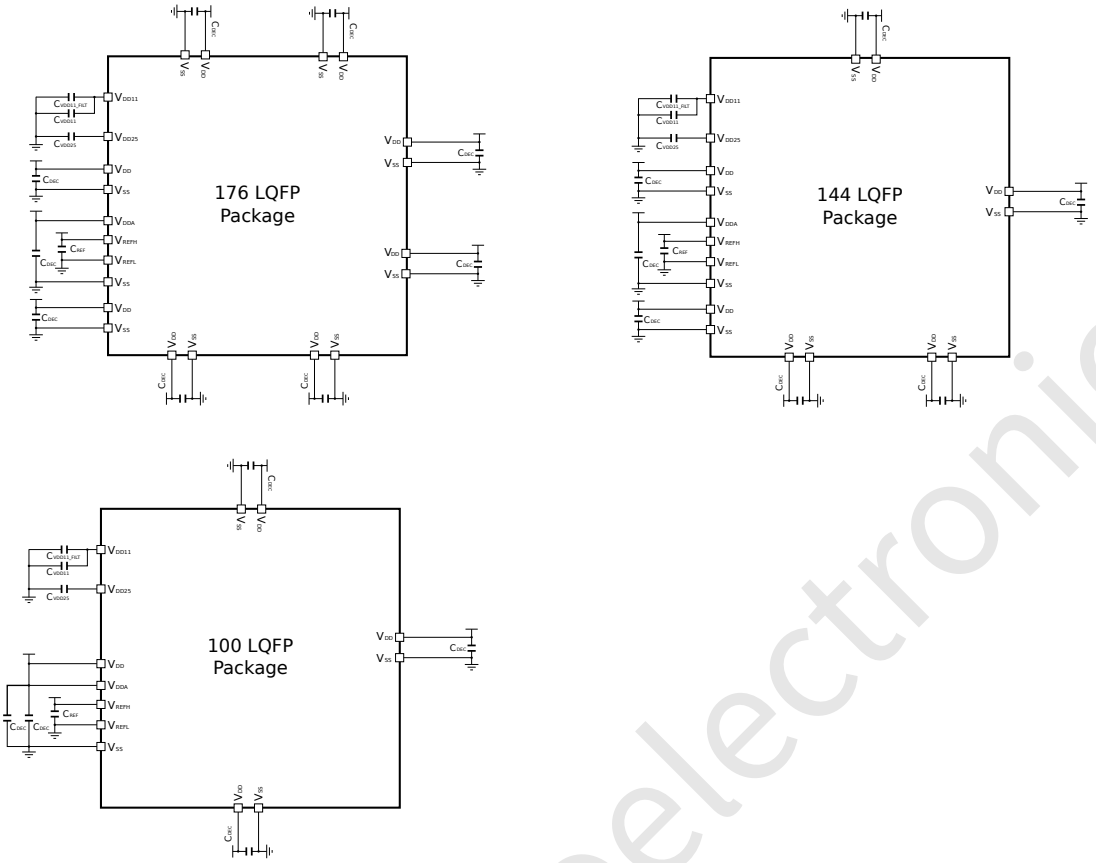


Figure 3: Pinout Decoupling

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF}[1,2]	ADC reference high decoupling capacitance	–	100	–	nF
C_{DEC0}[2,3]	Recommended decoupling capacitance	1	4.7	–	μF
C_{DEC1}[2,3]	Recommended decoupling capacitance	–	0.1	–	μF
C_{VDD11}	Internal PMC, LDO voltage	–	2.2	–	μF
C_{VDD11_FILT}	Internal PMC, LDO voltage, ripple filter	–	100	–	nF
C_{VDD25}	Internal PMC, LDO voltage	–	220	–	nF

1. For improved ADC performance it is recommended to use 1 nF X7R/C0G and 10 nF X7R ceramics in parallel.
2. The capacitors should be placed as close as possible to the VREFH/VREFL pins or corresponding VDD/VSS pins.
3. The requirement and value of of CDEC will be decided by the device application requirement.

6.2.6 POR, LVR and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	–	2.0	–	V	

Table 11 continued from previous page

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVD}	Falling low-voltage threshold	2.7	–	2.9	V	
V_{LVD_HYST}	LVD hysteresis	–	20	–	mV	

6.2.7 Power Mode Transition Operating Behaviors

Description	System clock	Core, bus frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	FIRC	48MHz	–	TBD	–
DEEPSLEEP -> ACTIVE	FIRC	48MHz	–	TBD	–
STANDBY -> ACTIVE	FIRC	48MHz	–	TBD	–
POWERDOWN -> ACTIVE	FIRC	48MHz	–	TBD	–
T_{POR}	FIRC(reset value)	48MHz	–	TBD	–

6.2.8 Power Consumption

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
ACTIVE	I_{DD_ACTIVE}	PLL	Running coremark in flash, all peripheral clock enabled. core @160MHz, slow bus @80MHz V_{DD}=5V	25 °C	–	TBD	–	mA
				125 °C	–	TBD	–	mA
			Running coremark in flash, all peripheral clock disabled. core @160MHz, slow bus @80MHz V_{DD}=5V	25 °C	–	TBD	–	mA
				125 °C	–	TBD	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @160MHz, slow bus @80MHz V_{DD}=5V	25 °C	–	TBD	–	mA
				125 °C	–	TBD	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @160MHz, slow bus @80MHz V_{DD}=5V	25 °C	–	TBD	–	mA
				125 °C	–	TBD	–	mA
SLEEP	I_{DD_SLEEP}	–	Sleep mode current, V_{DD}=5V	$\leq$ 25 °C	–	TBD	–	mA
				125 °C	–	TBD	–	mA
DEEPSLEEP	$I_{DD\_DEEPSLEEP}$	FIRC	Deepsleep mode current, V_{DD}=5V SIRC enabled	$\leq$ 25 °C	–	TBD	–	μA
				125 °C	–	TBD	–	μA
			Deepsleep mode current, V_{DD}=5V SIRC disabled	$\leq$ 25 °C	–	TBD	–	μA
				125 °C	–	TBD	–	μA
STANDBY	$I_{DD\_STANDBY}$	FIRC	Standby mode current, V_{DD}=5V SIRC enabled	$\leq$ 25 °C	–	TBD	–	μA
				125 °C	–	TBD	–	μA
			Standby mode current, V_{DD}=5V SIRC disabled	$\leq$ 25 °C	–	TBD	–	μA
				125 °C	–	TBD	–	μA
POWERDOWN	$I_{DD\_POWERDOWN}$	FIRC	Powerdown mode current, V_{DD}=5V SIRC enabled	$\leq$ 25 °C	–	TBD	–	μA
				125 °C	–	TBD	–	μA
			Powerdown mode current, V_{DD}=5V SIRC disabled	$\leq$ 25 °C	–	TBD	–	μA

Table 13 continued from previous page

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
				125 °C	–	TBD	–	μA

6.2.9 Power Sequence

Hardwares must follow sequence below to ensure that the chip is powered up properly.

1. VDD must be powered up first.
2. VDDA must be powered up later than or at the same time as VDD.
3. VREFH must be powered up later than or at the same time as VDDA.

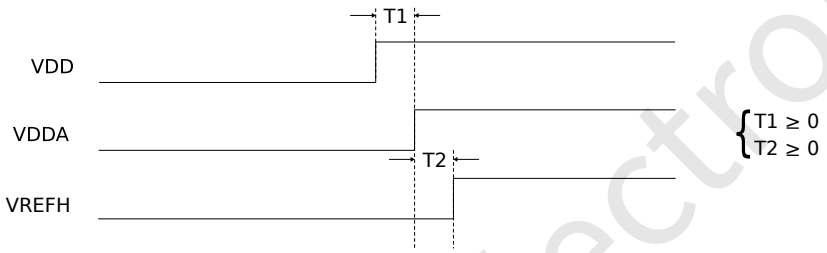


Figure 4: Power Sequence

6.2.10 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance.

6.3 AC Characteristics

6.3.1 Device Clock Specifications

Symbol	Description	Min.	Typ.	Unit	Notes
f_{core}	System and core clock	–	160	MHz	
f_{bus}	Fast bus clock	–	80	MHz	
	Slow bus clock	–	40	MHz	

6.3.2 I/O Electrical Characteristics

6.3.2.1 AC Electrical Characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and the rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

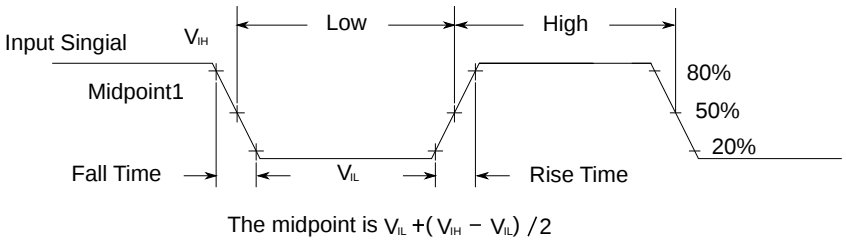


Figure 5: Input Signal Measurement Reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L = 30pF loads
- Normal drive strength

6.4 Peripheral Operating Requirements and Behaviors

6.4.1 FIRC (48MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{FIRC}	Fast internal reference frequency	–	48	–	MHz	
ACC_{FIRC}	FIRC frequency accuracy, factory trimmed, 25 °C	-0.2	–	0.2	%	
	FIRC frequence accuracy, factory trimmed, -40°C – 125°C	-1	–	1	%	
I_{FIRC}	FIRC operating current	–	160	–	μA	
$T_{Startup}$	Startup time	–	20	–	μs	

6.4.2 SIRC (2MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SIRC}	Slow internal reference frequency	–	2	–	MHz	
ACC_{SIRC}	SIRC frequency accuracy, factory trimmed, 25 °C	-1	–	1	%	
	SIRC frequency accuracy, factory trimmed, 0 °C – 85 °C	-5	–	5	%	
	SIRC frequence accuracy, factory trimmed, −40 °C – 125 °C	-5	–	5	%	
I_{SIRC}	SIRC operating current	–	25	–	μA	
$T_{Startup}$	Startup time	–	28	–	μs	

6.4.3 FXOSC (4~40MHz) Characteristics

The following diagram is Fast Crystal OSC circuit.

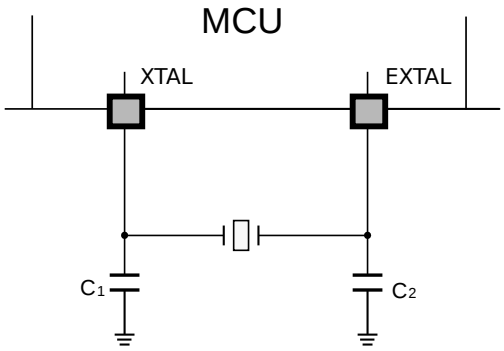


Figure 6: FXOSC Diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	TBD	–	TBD	V	
I_{DDOSC}	40MHz oscillator	–	TBD	–	mA	
V_{IH}	Input high voltage – EXTAL pin in external clock mode, V_{DD}=5V	TBD	–	TBD	V	
	Input high voltage – EXTAL pin in external clock mode, V_{DD}=3.3V	TBD	–	TBD	V	
V_{IL}	Input low voltage – EXTAL pin in external clock mode, V_{DD}=5V	TBD	–	TBD	V	
	Input low voltage – EXTAL pin in external clock mode, V_{DD}=3.3V	TBD	–	TBD	V	
$T_{FXOSCSU}$	FXOSC startup time (40MHz oscillator)	–	TBD	–	ms	
D_{FXOSC}	Duty of FXOSC (40MHz oscillator)	TBD	–	TBD	%	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	FXOSC internal feedback resistor	–	TBD	–	kΩ	
V_{PP}	Peak-to-peak amplitude of oscillation (40MHz oscillator)	–	TBD	–	V	

1. Depending on the oscillator manual, $C_L = (C_1 * C_2/(C_1 + C_2)) + C_S$. For crystal load balance, $C_1 = C_2$. C_S is parasitic capacitors, C_L is load capacitor of oscillator, calculate C_1 and C_2 according to this formula.

6.4.4 SXOSC(32.768 KHz) Characteristics

The following diagram is SXOSC circuit.

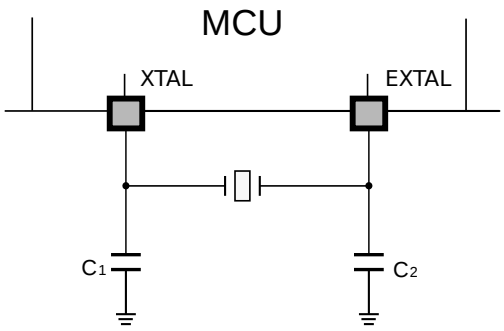


Figure 7: SXOSC Diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SXOSC}	Oscillator crystal frequency	–	32.768	–	KHz	
I_{DDOSC}	SXOSC oscillator	–	TBD	–	μA	
$T_{startup}$	SXOSC startup time (32.768KHz oscillator)	–	–	TBD	s	
D_{SXOSC}	Duty of SXOSC (32.768KHz oscillator)	TBD	TBD	TBD	%	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	SXOSC feedback resistor	–	TBD	–	MΩ	2
V_{PP}	Peak-to-peak amplitude of oscillation (32.768KHz oscillator)	–	TBD	–	V	

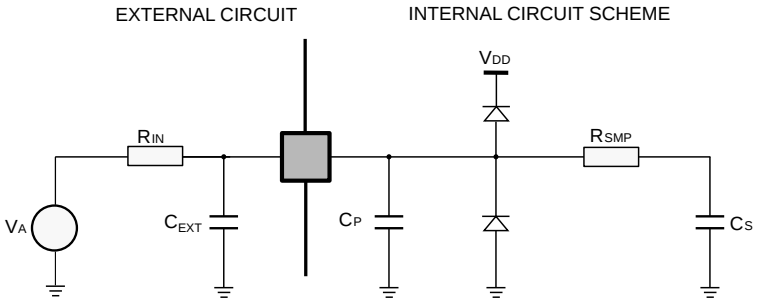
1. Depending on the oscillator manual, $C_L = (C_1 * C_2/(C_1 + C_2)) + C_S$. For crystal load balance, $C_1 = C_2$. C_S is parasitic capacitors, C_L is load capacitor of oscillator, calculate C_1 and C_2 according to this formula.
2. The feedback resistor is internal

6.4.5 PLL Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{ref}	PLL reference frequency range	8	–	96	MHz	
F_{input}	PLL input frequency	8	–	48	MHz	5
F_{vco}	VCO frequency	180	–	600	MHz	
F_{out}	Out frequency	90	–	300	MHz	1, 4
N_{pre}	Reference clock predivider divider	1	–	16		2
N_{div}	VCO feedback divider	10	–	64		3

1. PLL OUT divider is 2, $F_{out} = F_{vco}/2$
2. PLL clock pre-divider is from 1 to 16. If need to re-configure. It is recommended to switch to other clock source, then disable PLL, and configure PLL predivider, switch to PLL, and enable it finally.
3. PLL clock feedback divider is from 10 to 63. It is recommended to switch to other clock source, then disable PLL, and configure PLL predivider, switch to PLL, and enable it finally.
4. $F_{out} = \frac{F_{ref}}{2*N_{pre}} * N_{div}$
5. $F_{input} = \frac{F_{ref}}{N_{pre}}$

6.4.6 ADC Characteristics



Note: R_{IN} is the internal resistance of signal source.

Figure 8: ADC Circuit

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage		2.97	5.0	5.5	V	1
I_{DDA}	Analog supply current		–	1.19	–	mA	
ΔV_{DDA}	V_{DD} - V_{DDA}		-100	–	100	mV	
V_{REFH}	Reference voltage		2.97	–	V_{DDA}	V	
I_{REFH}	Reference current		–	494.95	–	μA	
V_{IN}	Input voltage		0	–	V_{REFH}	V	
R_{SMP}	Sampling switch impedance		5	–	154	Ω	
C_{EXT}	External capacitance		–	30	–	nF	
C_P	Pin Capacitance		–	3	–	pF	
C_S	Sampling capacitance		–	6.3	–	pF	

1. For 2Msps, ADC only supports 4V ~5.5V.

Symbol	Description	Test condition[1]	Min.	Typ.	Max.	Unit	Notes
$T_{STARTUP}$	Analog startup time		–	2	–	μs	
T_{SAMPLE}	Sampling time	ADC functional clock is 16MHz	4	–	–	cycles	2
T_{CONV_12BIT}	Total conversion time with sample	ADC functional clock is 16MHz and select 12-bit resolution	–	16	–	cycles	2
T_{CONV_10BIT}	Total conversion time with sample	ADC functional clock is 16MHz and select 10-bit resolution	–	14	–	cycles	2

Table 21 continued from previous page

Symbol	Description	Test condition[1]	Min.	Typ.	Max.	Unit	Notes
T_{CONV_8BIT}	Total conversion time with sample	ADC functional clock is 16MHz and select 8-bit resolution	–	12	–	cycles	2
T_{CONV_6BIT}	Total conversion time with sample	ADC functional clock is 16MHz and select 6-bit resolution	–	10	–	cycles	2

1. Theses parameters of this table can be configured by register, please refer to Reference Manual for details.
2. For 2Msps ADC, function clock is configured to 32MHz.

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
DNL	Differential nonlinear	12-bit resolution	–	TBD	–	LSB
INL	Integer nonlinear	12-bit resolution	–	TBD	–	LSB
E_{GAIN}	Gain error	12-bit resolution	–	TBD	–	LSB
E_{OFFSET}	Offset error	12-bit resolution	–	TBD	–	LSB
ENOB	Effective number bits	12-bit resolution	–	TBD	TBD	Bits
SINAD	Signal-to-noise-and-distortion ratio	12-bit resolution	–	TBD	TBD	dB
ACC_{tempS}	Temperature sensor accuracy		10		-10	°C
K[1]	Slope of temperature and voltage curve	ADC sampling frequncy @ 500kHz		546.4		

1. T = C - K*V, see Reference Manual for details.

6.4.7 ACMP Characteristics

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{ACMP}[1]	Analog supply voltage		2.97	5.0	5.5	V	
I_{ACMP}	Analog supply current	hi_pwr=0	2.5	4.4	24.5	μA	
		hi_pwr=1	77	127	209	μA	
$V_{INOFFSET}$	Analog input offset voltage		–	5	–	mV	
V_{IN}	Analog input voltage		0	–	V_{DDA}	V	
V_{HYST0}	Analog comparator hysteresis 0		–	20	–	mV	
V_{HYST1}	Analog comparator hysteresis 1		–	40	–	mV	

1. V_{ACMP} connects to VDD.

6.4.8 NVM Specifications

6.4.8.1 Flash Command Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T_{pgm}	Program execution time	47	–	54	μs	
T_{sector_erase}	Sector erase execution time	8.5	–	20.5	ms	
T_{block_erase}	Block erase execution time	9	–	21	ms	

6.4.8.2 Flash High Voltage Current Behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_PGM}	Average current adder during high voltage flash programming operation	–	TBD	TBD	mA	
I_{DD_ERS}	Average current adder during high voltage flash erase operation	–	TBD	TBD	mA	

6.4.8.3 Reliability Specifications

Symbol	Description	Min.	Max.	Unit	Notes
$t_{nvmretp}$	Data retention	10	–	years	
$t_{nvmcycp}$	Cycling endurance	100K	–	cycles	

6.4.9 Debug Module Electrical

6.4.9.1 SWD Electrical Specifications

Table 27: SWD Full Voltage Range Electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

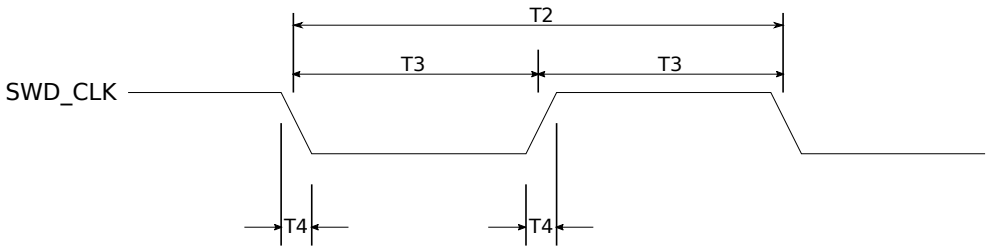


Figure 9: SWD Clock Timing

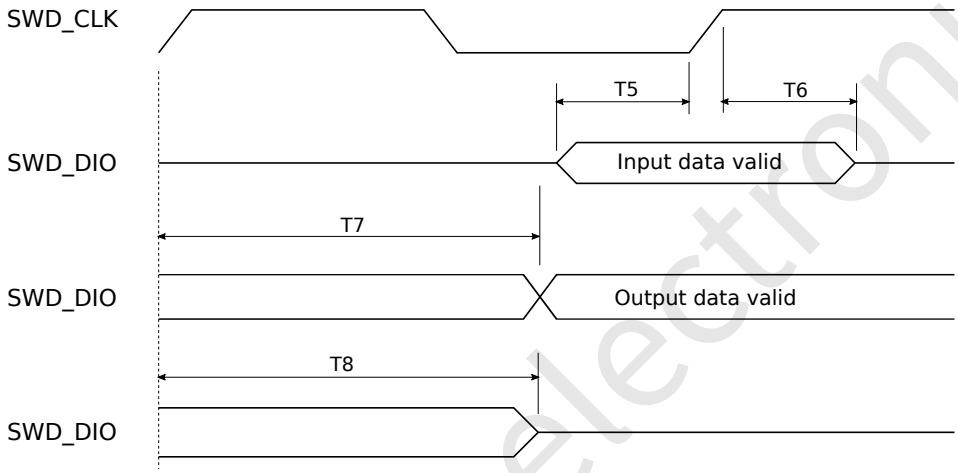


Figure 10: SWD Data Timing

6.4.9.2 JTAG Electrical Specifications

Table 28: JTAG Electrical Specifications

Symbol	Description	Active				Unit
		5.0V IO		3.3V IO		
		Min.	Max.	Min.	Max.	
J1	TCLK frequency					MHz
	Boundary Scan	–	20	–	20	
	JTAG	–	20	–	20	
J2	TCLK cycle period	1/J1	–	1/J1	–	ns
J3	TCLK clock pulse width					ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG					
J4	TCLK rise and fall times	–	1	–	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	–	5	–	ns
J6	Boundary scan input data hold time after TCLK rise	5	–	5	–	ns
J7	TCLK low to boundary scan output data valid	–	28	–	32	ns
J8	TCLK low to boundary scan output data invalid	0	–	0	–	ns

Table 28 continued from previous page

Symbol	Description	Active				Unit
		5.0V IO		3.3V IO		
		Min.	Max.	Min.	Max.	
J9	TCLK low to boundary scan output high-Z	–	28	–	32	ns
J10	TMS, TDI input data setup time to TCLK rise	3	–	3	–	ns
J11	TMS, TDI input data hold time after TCLK rise	2	–	2	–	ns
J12	TCLK low to TDO data valid	–	28	–	32	ns
J13	TCLK low to TDO data invalid	0	–	0	–	ns
J14	TCLK low to TDO high-Z	–	28	–	28	ns

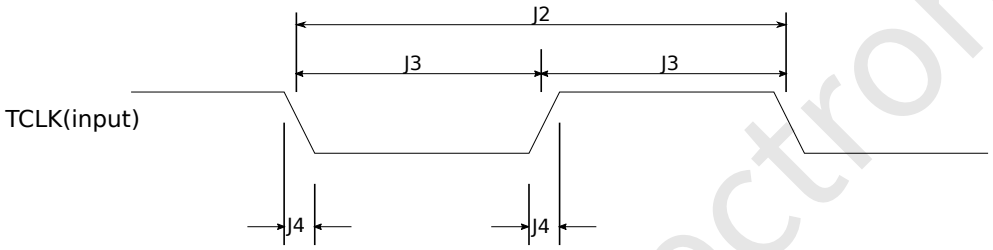


Figure 11: JTAG Clock Timing

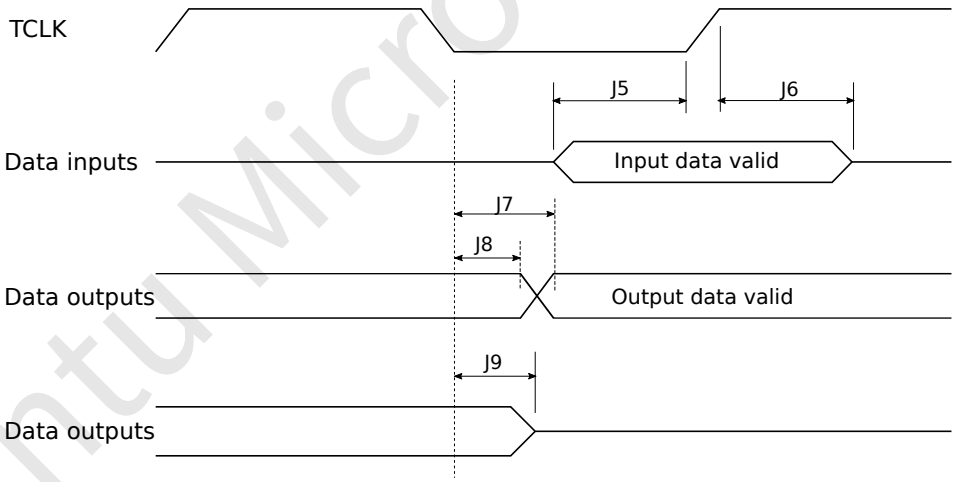


Figure 12: JTAG Data Timing

6.5 Thermal Attributes

Table 29: Thermal Characteristics

Package Family	Package Type	Thermal Resistance JA (°C/W)
LQFP	LQFP100L	57
	LQFP144L	45
	LQFP176L	33

7 Pinouts

7.1 IO Signal Description

The pinouts signal description is as follows:

Table 30: Pinmux Table

176 LQFP	144 LQFP	100 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
1			PTA_18		PTA_18	MPWM0_CH0	UART1_TX	SPI1_SOUT	MPWM0_CH8	ADC1_EXP_SEL3									
2			PTA_19		PTA_19	MPWM0_CH1	UART1_RX	SPI1_SCK		ADC1_EXP_SEL2									
3			PTA_20		PTA_20	MPWM0_CH2		SPI1_SIN		ADC1_EXP_SEL1									
4	1	1	PTE_16	ADC0_S28	PTE_16	UART3_TX	SPI2_SIN	eTMR2_CH7			TMU_OUT7				UART1_RTS				
5	2	2	PTE_15	ADC0_S27	PTE_15	UART3_RX	SPI2_SCK	eTMR2_CH6			TMU_OUT6				UART1_CTS				
6			PTA_21		PTA_21	MPWM0_CH3		SPI1_PCS0		ADC1_EXP_SEL0		SPI2_PCS2							
7	3	3	VDD11	VDD11															
8	4	4	VDD25	VDD25															
9			PTA_22		PTA_22	MPWM0_CH4		SPI1_PCS1											
10	5	5	PTE_11	ADC0_S30	PTE_11	SPI2_PCS0	lpTMR0_ALT1	eTMR2_CH5	UART3_TX	ETM_TRACE_D0	TMU_OUT5	UART4_TX							
11	6	6	PTE_10	ADC0_S29	PTE_10	SCU_CLKOUT	SPI2_PCS1	eTMR2_CH4	UART3_RX		TMU_OUT4	UART4_RX		SPI3_SIN					
12	7	7	PTE_13	ADC1_S_EXP	PTE_13	MPWM0_CH5	SPI2_PCS2	eTMR2_FLT0	SPI2_PCS0				MPWM0_CH10			eTMR3_CH5			
13			PTA_23		PTA_23	MPWM0_CH6													
14	8	8	PTE_5		PTE_5	TCLK_IN2	eTMR2_QD_PHA	eTMR2_CH3	CAN0_TX	eTMR3_CH5	EWDG_IN			ADC0_EXP_SEL0					
15	9	9	PTE_4		PTE_4	ETM_TRACE_D1	eTMR2_QD_PHB	eTMR2_CH2	CAN0_RX	eTMR3_CH4	EWDG_OUT_b	SPI0_PCS0	eTMR3_CH7	ADC0_EXP_SEL1	SPI1_PCS1				
16			PTA_24		PTA_24	MPWM0_CH7								MPWM0_CH0	ADC0_EXP_SEL2				
17	10		PTA_25		PTA_25	MPWM0_CH8									ADC0_EXP_SEL3				
18	11	10	VDD	VDD															
19	12		VSS	VSS															
20	13	11	VDDA	VDDA															
21	14	12	VREFH	VREFH															
22	15	13	VREFL	VREFL															
23	16	14	VSS	VSS															
24	17	15	PTB_7	EXTAL	PTB_7	I2C0_SCL		SPI3_SCK			TMU_OUT2								
25	18	16	PTB_6	XTAL	PTB_6	I2C0_SDA		SPI3_SIN			TMU_OUT1								
26	19		PTA_26		PTA_26	MPWM0_CH9	SPI1_PCS0	SPI0_PCS0						MPWM0_CH1					
27	20	17	PTE_14		PTE_14	eTMR0_FLT1		eTMR2_FLT1	SCU_CLKOUT			CAN4_RX			eTMR2_CH3	UART5_TX			
28	21	18	PTE_3		PTE_3	eTMR0_FLT0	SPI1_SIN	eTMR2_FLT0	SPI3_SOUT	TMU_IN6	ACMP0_OUT	CAN4_TX	eTMR2_CH3	UART2_RTS		UART5_RX			
29	22		PTA_27		PTA_27	MPWM0_CH10	SPI1_SOUT	UART0_TX	CAN0_TX						MPWM0_CH2				
30	23	19	PTE_12		PTE_12	eTMR0_FLT3	UART2_TX		SPI3_PCS0		UART2_RTS		eTMR3_CH5		ACMP0_ACTIVE	CAN5_TX			
31	24		PTA_28		PTA_28	MPWM0_CH11	SPI1_SCK	UART0_RX	CAN0_RX	ADC0_EXP_SEL3				MPWM0_CH3					
32	25	20	PTD_17		PTD_17	eTMR0_FLT2	UART2_RX		SPI3_PCS0	ADC0_EXP_SEL2		SPI5_PCS0	eTMR2_CH2		CAN5_RX	eTMR2_CH2			
33	26		PTA_29		PTA_29	MPWM0_CH12		UART2_TX	SPI1_SIN	ADC0_EXP_SEL1				MPWM0_CH4					
34	27		PTA_30		PTA_30	MPWM0_CH13	UART2_RX	SPI0_SOUT		ADC0_EXP_SEL0				MPWM0_CH5	SPI1_SOUT				
35	28	21	PTD_16	EXTAL32	PTD_16	eTMR0_CH1	CAN4_TX	SPI0_SIN	ACMP0_ACTIVE	ETM_TRACE_D2	ETM_TRACE_CLKOUT	UART2_RTS	MPWM0_CH7						
36	29	22	PTD_15	XTAL32	PTD_15	eTMR0_CH0	CAN4_RX	SPI0_SCK	SPI3_PCS1	ETM_TRACE_D3					CAN3_RX	MPWM0_CH6			
37	30	23	PTE_9		PTE_9	eTMR0_CH7	SPI1_SCK	I2C2_SDA			SCU_CLKOUT	SPI5_SOUT	UART2_CTS		CAN3_TX	MPWM0_CH5			

Table 30 continued from previous page

176 LQFP	144 LQFP	100 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
38	31		VSS	VSS															
39	32		VDD	VDD															
40	33		PTA_31		PTA_31	MPWM0_CH14		SPI0_PCS1			TMU_OUT8			MPWM0_CH6				MPWM0_CH4	
41	34	24	PTD_14		PTD_14	eTMR2_CH5	UART1_TX	I2C0_SCL				SPI5_SCK	SPI5_PCS3	SCU_CLKOUT	ACMP0_ACTIVE				
42	35	25	PTD_13		PTD_13	eTMR2_CH4	UART1_RX	I2C0_SDA			RTC_CLKOUT	SPI5_SIN	SPI5_PCS2					MPWM0_CH5	
43	36		PTB_18	ADC0_S16	PTB_18	MPWM0_CH15		SPI1_PCS1			TMU_OUT9	UART2_TX		MPWM0_CH7				MPWM0_CH6	
44			PTB_19		PTB_19	MPWM0_CH7				MPWM0_CH15	TMU_OUT10	UART2_RX							
45	37		PTB_20	ADC0_S17	PTB_20	UART3_TX		CAN5_RX	I2C1_SDA	MPWM1_CH0					MPWM0_CH8				
46	38		PTB_21	ADC0_S18	PTB_21	UART3_RX		CAN5_TX	I2C1_SCL	MPWM1_CH1					MPWM0_CH9				
47	39	26	PTE_8	ACMP0_IN3	PTE_8	eTMR0_CH6	SPI5_PCS1	I2C2_SCL			MPWM0_CH9	SPI3_PCS1				SENT0_RX_IN0			
48	40	27	PTB_5		PTB_5	eTMR0_CH5	SPI0_PCS1	SPI0_PCS0	SCU_CLKOUT	TMU_IN0			MPWM0_CH3	I2C2_SCL		SENT0_RX_IN1			
49	41	28	PTB_4		PTB_4	eTMR0_CH4	SPI0_SOUT			TMU_IN1			MPWM0_CH2	SCU_CLKOUT					
50	42	29	PTC_3	ADC0_S11 /ACMP0_IN4	PTC_3	eTMR0_CH3	CAN0_TX	UART0_TX	SPI4_PCS0										
51	43	30	PTC_2	ADC0_S10 /ACMP0_IN5	PTC_2	eTMR0_CH2	CAN0_RX	UART0_RX	SPI4_SCK	ETM_TRACE_ CLKOUT			SPI0_PCS2	SPI3_PCS2					
52	44	31	PTD_7	ACMP0_IN6	PTD_7	UART2_TX	eTMR0_CH3	eTMR2_FLT3	SPI4_SIN	ETM_TRACE_ D0					SPI3_PCS3	SPI0_PCS3			
53	45	32	PTD_6	ACMP0_IN7	PTD_6	UART2_RX	eTMR0_CH2	eTMR2_FLT2	SPI4_SOUT		SPI0_PCS0				MPWM0_CH4				
54	46	33	PTD_5		PTD_5	eTMR2_CH3	lpTMR0_ALT2	eTMR2_FLT1	SPI4_PCS1	TMU_IN7	SPI0_PCS1				eTMR0_CH2				
55	47	34	PTD_12		PTD_12	eTMR2_CH2		ETM_TRACE_ D1		SPI0_SOUT				UART2_RTS		SPI5_SIN			
56	48	35	PTD_11		PTD_11	eTMR2_CH1	eTMR2_QD_PHA	ETM_TRACE_ D2		SPI0_SCK				UART2_CTS			SPI5_SOUT		
57	49	36	PTD_10		PTD_10	eTMR2_CH0	eTMR2_QD_PHB	ETM_TRACE_ D3	SPI0_SIN						MPWM0_CH2		SPI5_SCK	SCU_CLKOUT	
58	50	37	VSS	VSS															
59	51	38	VDD	VDD															
60	52	39	PTC_1	ADC0_S9	PTC_1	eTMR0_CH1	SPI2_SOUT	CAN3_TX	UART5_TX	eTMR1_CH7		CAN3_RX							
61	53	40	PTC_0	ADC0_S8	PTC_0	eTMR0_CH0	SPI2_SIN	CAN3_RX	UART5_RX	eTMR1_CH6		CAN3_TX							
62	54	41	PTD_9		PTD_9	UART4_TX		eTMR2_FLT3		eTMR1_CH5				I2C1_SCL	UART6_TX				
63	55	42	PTD_8		PTD_8	UART4_RX		eTMR2_FLT2		eTMR1_CH4		SPI3_SOUT		I2C1_SDA	UART6_RX				
64	56	43	PTC_17	ADC0_S15	PTC_17	eTMR1_FLT3	CAN2_TX	SPI4_PCS0	eTMR2_CH1		I2C1_SCL	SPI3_SCK							
65	57	44	PTC_16	ADC0_S14	PTC_16	eTMR1_FLT2	CAN2_RX	SPI4_SCK	eTMR2_CH0		I2C1_SDA	SPI3_SIN	MPWM0_CH1			UART2_RX			
66	58		PTB_22	ADC0_S19	PTB_22	MPWM0_CH10	SPI3_PCS1		UART1_TX			CAN2_RX		CAN1_TX					
67	59	45	PTC_15	ADC0_S13	PTC_15	eTMR1_CH3	SPI2_SCK	SPI4_SIN	UART4_TX	TMU_IN8	I2C1_SCL	CAN2_TX		CAN1_RX	UART2_TX				
68	60		PTB_23	ADC0_S20	PTB_23	MPWM1_CH3	UART1_RX				CAN1_RX			MPWM0_CH11					
69			PTB_24		PTB_24	MPWM0_CH12					CAN1_TX								
70	61	46	PTC_14	ADC0_S12	PTC_14	eTMR1_CH2	SPI2_PCS0	SPI4_SOUT	UART4_RX	TMU_IN9	eTMR3_CH4			CAN2_RX					
71	62		PTB_25	ADC0_S21	PTB_25	MPWM1_CH5		SPI4_PCS1	SPI2_PCS0				MPWM0_CH13	CAN2_TX					
72			PTB_26		PTB_26	MPWM0_CH14													
73	63	47	PTB_3	ADC0_S7	PTB_3	eTMR1_CH1	SPI0_SIN	eTMR1_QD_PHA	CAN4_TX	TMU_IN2					SPI2_SOUT				
74	64		PTB_27	ADC0_S22	PTB_27		MPWM1_CH7		SPI2_SOUT			UART5_TX	MPWM0_CH15					MPWM0_CH0	
75	65		PTB_28	ADC0_S23	PTB_28		MPWM1_CH8		SPI2_SIN				UART5_RX					MPWM0_CH1	
76	66		VSS	VSS															
77	67		VDD	VDD															
78	68	48	PTB_2	ADC0_S6	PTB_2	eTMR1_CH0	SPI0_SCK	eTMR1_QD_PHB		TMU_IN3			CAN4_RX			SPI2_SIN		MPWM0_CH2	
79	69		PTB_29		PTB_29	MPWM1_CH9			SPI2_SCK			UART6_TX						MPWM0_CH3	
80			PTB_30		PTB_30	MPWM1_CH10												MPWM0_CH4	
81	70	49	PTC_13		PTC_13	eTMR3_CH7	eTMR2_CH7		UART2_RTS					ADC0_EXP_ SEL2	eTMR3_CH3				
82			PTB_31		PTB_31	MPWM1_CH11												MPWM0_CH5	

Table 30 continued from previous page

176 LQFP	144 LQFP	100 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
83			PTC_18		PTC_18	MPWM1_CH12						UART6_RX						MPWM0_CH6	
84	71	50	PTC_12		PTC_12	eTMR3_CH6	eTMR2_CH6	SPI2_PCS1	UART2_CTS					ADC0_EXP_SEL1	eTMR3_CH2				
85	72		PTC_19		PTC_19	MPWM1_CH13			SPI2_PCS1			UART7_TX						MPWM0_CH7	
86			PTC_20		PTC_20	MPWM1_CH14						UART7_RX						MPWM0_CH8	
87			PTC_21		PTC_21	MPWM1_CH15												MPWM0_CH9	
88			PTC_22		PTC_22							eTMR1_CH0						MPWM0_CH10	
89	73		PTC_23		PTC_23	SPI0_SCK												MPWM0_CH11	
90			PTC_24		PTC_24	MPWM0_CH0	eTMR3_CH0											MPWM0_CH12	
91			PTC_25		PTC_25	MPWM0_CH1	eTMR3_CH1		SPI4_PCS1									MPWM0_CH13	
92	74	51	PTC_11		PTC_11	eTMR3_CH5	MPWM0_CH2	CAN5_TX		TMU_IN10	ADC0_EXP_SEL0		CAN5_RX		eTMR3_CH1	SPI4_SOUT			
93			PTC_26		PTC_26	MPWM0_CH3	eTMR3_CH3				SPI4_SIN		CAN5_RX					MPWM0_CH14	
94	75	52	PTC_10	ADC1_S27	PTC_10	eTMR3_CH4		CAN5_RX	SPI4_PCS0	TMU_IN11	eTMR3_CH0	eTMR0_CH6		CAN5_TX		SPI2_PCS1			
95	76		PTC_27		PTC_27	MPWM0_CH4					SPI4_SCK	CAN5_TX			eTMR3_CH4			MPWM0_CH15	
96	77	53	PTB_1	ADC0_S5	PTB_1	UART0_TX	SPI0_SOUT	TCLK_IN0	CAN0_TX	MPWM0_CH5	I2C0_SCL			eTMR3_CH5		eTMR0_CH7		MPWM0_CH0	
97	78	54	PTB_0	ADC0_S4	PTB_0	UART0_RX	SPI0_PCS0	lpTMR0_ALT3	CAN0_RX	MPWM0_CH6	I2C0_SDA			eTMR3_CH6		eTMR0_CH3		MPWM0_CH1	
98	79		PTC_28		PTC_28	MPWM0_CH7			I2C1_SCL			CAN3_TX			eTMR3_CH7				
99	80	55	PTC_9		PTC_9	UART1_TX	eTMR1_FLT1	MPWM0_CH8	CAN4_TX	SPI0_SIN	I2C0_SDA	UART0_RTS	CAN1_RX	MPWM0_CH0			SPI5_PCS1	MPWM0_CH2	
100	81	56	PTC_8	DAC0_OUT	PTC_8	UART1_RX	eTMR1_FLT0	MPWM0_CH9	CAN4_RX	SPI0_SCK	I2C0_SCL	UART0_CTS	CAN1_TX	MPWM0_CH1			SPI5_PCS0	MPWM0_CH3	
101	82		PTC_29		PTC_29	MPWM0_CH10			I2C1_SDA			CAN3_RX	MPWM0_CH2						
102	83	57	PTA_7	ADC0_S3	PTA_7	eTMR0_FLT2	MPWM0_CH11	RTC_CLKIN	I2C2_SCL		UART1_RTS	UART3_TX	SPI0_PCS1	MPWM0_CH3	CAN0_TX			SPI5_SCK	
103	84		PTC_30		PTC_30	MPWM0_CH12		I2C1_SDA				CAN4_TX	MPWM0_CH4						
104	85	58	PTA_6	ADC0_S2	PTA_6	eTMR0_FLT1	SPI1_PCS1	MPWM0_CH13	I2C2_SDA	SPI3_PCS1	UART1_CTS	UART3_RX	CAN0_RX	MPWM0_CH5			SPI5_SIN		
105	86		PTC_31		PTC_31	MPWM0_CH14		I2C1_SDA					CAN4_RX		MPWM0_CH6				
106	87	59	PTE_7		PTE_7	eTMR0_CH7	eTMR3_FLT0			SPI3_SCK			UART4_RX		SPI5_SOUT				
107	88		PTD_18	ADC1_S16	PTD_18	MPWM0_CH15	CAN5_TX	I2C1_SCL	I2C1_SDA										
108	89		PTD_19	ADC1_S17	PTD_19	MPWM1_CH0	CAN5_RX		I2C1_SCL										
109	90	60	VSS	VSS															
110	91	61	VDD	VDD															
111	92	62	PTA_17		PTA_17	eTMR0_CH6	eTMR3_FLT0	EWDG_OUT_b		SPI3_SOUT	ADC1_EXP_SEL0	UART4_TX							
112	93	63	PTB_17	ADC1_S26	PTB_17	eTMR0_CH5	SPI1_PCS3			SPI3_PCS0		UART4_RX		eTMR3_CH7					
113			PTD_20	ADC1_S31	PTD_20	MPWM0_CH9			SPI1_PCS2	SPI3_SIN									
114	94	64	PTB_16	ADC1_S15	PTB_16	eTMR0_CH4	SPI1_SOUT	UART4_TX											
115	95	65	PTB_15	ADC1_S14	PTB_15	eTMR0_CH3	SPI1_SIN			UART7_TX									
116	96	66	PTB_14	ADC1_S9	PTB_14	eTMR0_CH2	SPI1_SCK			UART7_RX									
117			PTD_21		PTD_21	MPWM0_CH10													
118	97	67	PTB_13	ADC1_S8	PTB_13	eTMR0_CH1	eTMR3_FLT1	CAN2_TX				SPI3_PCS2							
119	98	68	PTB_12	ADC1_S7	PTB_12	eTMR0_CH0	eTMR3_FLT2	CAN2_RX				SPI3_PCS3							
120	99		PTD_22	ADC1_S18	PTD_22		MPWM1_CH3		MPWM0_CH12				MPWM0_CH11						
121	100	69	PTD_4	ADC1_S6	PTD_4	eTMR0_FLT3	eTMR3_FLT3		MPWM0_CH13		SPI5_PCS0		MPWM0_CH15	SPI1_PCS1		SPI5_PCS2			
122	101	70	PTD_3	ADC1_S3	PTD_3	eTMR3_CH5	SPI1_PCS0	I2C1_SCL	CAN5_TX	TMU_IN4	CORE_NMI_b		MPWM0_CH14	UART3_RX					
123	102	71	PTD_2	ADC1_S2	PTD_2	eTMR3_CH4	SPI1_SOUT	I2C1_SDA	CAN5_RX	TMU_IN5	SPI5_SOUT		MPWM0_CH13	UART3_TX					
124	103		PTD_23	ADC1_S19	PTD_23		SPI3_PCS0	MPWM1_CH4	MPWM0_CH14				MPWM0_CH12						
125	104	72	PTA_3	ADC1_S1	PTA_3	eTMR3_CH1	I2C0_SCL	EWDG_IN		UART0_TX	SPI5_SCK		MPWM0_CH12	SPI1_SCK					
126	105	73	PTA_2	ADC1_S0	PTA_2	eTMR3_CH0	I2C0_SDA	EWDG_OUT_b		UART0_RX	SPI5_SIN		MPWM0_CH11				SPI1_SIN		
127	106		PTD_24	ADC1_S20	PTD_24	MPWM1_CH5							MPWM0_CH13						
128	107	74	PTB_11	ADC1_S30	PTB_11	eTMR3_CH3	UART5_TX					SPI4_SIN	MPWM0_CH10						
129			VDD	VDD															
130			VSS	VSS															
131	108	75	PTB_10	ADC1_S29	PTB_10	eTMR3_CH2	UART5_RX			I2C0_SDA		SPI4_SCK	MPWM0_CH9						
132			PTD_25		PTD_25	MPWM0_CH14			ADC1_EXP_SEL1										
133	109	76	PTB_9	ADC0_S25	PTB_9	MPWM0_CH8	eTMR3_CH1			I2C0_SCL		SPI4_SOUT							
134			PTD_26		PTD_26	MPWM0_CH15			ADC1_EXP_SEL2	SPI5_SCK									
135	110		PTD_27	ADC1_S21	PTD_27		MPWM1_CH8			SPI5_SOUT									

Table 30 continued from previous page

176 LQFP	144 LQFP	100 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
136	111	77	PTB_8	ADC0_S24	PTB_8	eTMR3_CH0				SPI0_PCS5		SPI4_PCS0	MPWM0_CH7						
137	112		PTD_28	ADC1_S22	PTD_28		MPWM1_CH9			SPI5_SIN									
138	113	78	PTA_1	ADC0_S1 /ACMP0_IN1	PTA_1	eTMR1_CH1	UART5_TX	I2C0_SDA	eTMR1_QD_PHA	SPI0_PCS6	TMU_OUT0	SPI4_PCS1	UART0_RTS						
139	114		PTD_29	ADC1_S23	PTD_29	MPWM1_CH10			SPI4_PCS1	SPI5_PCS2									
140	115	79	PTA_0	ADC0_S0 /ACMP0_IN0	PTA_0	eTMR2_CH1	UART5_RX	I2C0_SCL	eTMR2_QD_PHA	SPI0_PCS7	TMU_OUT3	SPI4_PCS2	UART0_CTS	eTMR3_CH0					
141	116		PTD_30		PTD_30	MPWM1_CH11				SPI5_PCS3	ADC1_EXP_SEL3								
142			PTD_31		PTD_31	MPWM1_CH12													
143	117	80	PTC_7	ADC1_S5	PTC_7	UART1_TX	CAN1_TX	eTMR3_CH3	eTMR3_CH7	eTMR1_QD_PHA		I2C1_SCL		SPI0_PCS0		CAN2_TX			
144	118	81	PTC_6	ADC1_S4	PTC_6	UART1_RX	CAN1_RX	eTMR3_CH2	eTMR3_CH6	eTMR1_QD_PHB		I2C1_SDA		SPI0_PCS1		CAN2_RX	SPI1_PCS1	MPWM1_CH9	
145			PTE_17		PTE_17	MPWM1_CH13													
146	119	82	PTA_16	ADC1_S13	PTA_16	eTMR1_CH3	SPI1_PCS2	SPI0_PCS4	UART6_TX			SPI4_PCS3						MPWM1_CH0	
147			PTE_18		PTE_18	MPWM1_CH14													
148	120	83	PTA_15	ADC1_S12	PTA_15	eTMR1_CH2	SPI0_PCS3	SPI2_PCS3	UART6_RX	SPI5_PCS0								MPWM1_CH1	
149	121	84	PTE_6	ADC1_S11	PTE_6	SPI0_PCS2		eTMR3_CH7	UART1_RTS			MPWM0_CH6		ETM_TRACE_ D2	ETM_TRACE_ CLKOUT			MPWM1_CH2	
150	122	85	PTE_2	ADC1_S10	PTE_2	SPI0_SOUT	lpTMR0_ALT3	eTMR3_CH6	UART1_CTS			eTMR0_CH3	MPWM0_CH0		ETM_TRACE_ D3			MPWM1_CH3	
151	123	86	VSS	VSS															
152	124	87	VDD	VDD															
153	125		PTE_19		PTE_19	eTMR2_CH6	MPWM1_CH15	SPI1_PCS4		SPI0_SCK									
154	126		PTE_20		PTE_20	MPWM0_CH0		SPI1_PCS3		SPI0_SIN			eTMR3_CH0						
155	127	88	PTA_14	ADC1_S28	PTA_14	eTMR0_FLT0	eTMR3_FLT1	EWDG_IN		eTMR1_FLT0			eTMR3_CH4	SPI1_PCS3	SPI5_PCS1			MPWM1_CH0	
156	128		PTE_21		PTE_21	MPWM0_CH1				SPI4_SIN			eTMR3_CH1			ADC1_EXP_SEL3		MPWM1_CH1	
157	129		PTE_22		PTE_22	MPWM0_CH2				SPI4_SCK			eTMR3_CH2			ADC1_EXP_SEL2		MPWM1_CH2	
158	130	89	PTA_13	ADC1_S25	PTA_13	eTMR1_CH7	CAN1_TX	SPI3_PCS0		eTMR2_QD_PHA		SPI1_PCS4	eTMR3_CH3					MPWM1_CH3	
159	131		PTE_23		PTE_23	MPWM0_CH3	CAN1_RX			SPI4_PCS0			eTMR3_CH3					MPWM1_CH4	
160	132		PTE_24		PTE_24	MPWM0_CH4	CAN2_TX			SPI4_PCS1			eTMR3_CH4					MPWM1_CH5	
161	133		PTE_25		PTE_25	MPWM0_CH5	CAN2_RX			SPI4_SOUT			eTMR3_CH5					MPWM1_CH6	
162	134	90	PTA_12	ADC1_S24	PTA_12	eTMR1_CH6	CAN1_RX	SPI3_SCK	I2C1_SDA	eTMR2_QD_PHB			SPI1_PCS5	eTMR3_CH2		SCU_CLKOUT	SENT0_RX_IN0	MPWM1_CH7	
163	135	91	PTA_11		PTA_11	eTMR1_CH5	CAN1_TX	SPI3_SIN	ACMP0_ACTIVE	SPI1_PCS0	TMU_OUT8		eTMR3_CH1				SENT0_RX_IN1	MPWM1_CH8	
164	136	92	PTA_10		PTA_10	eTMR1_CH4	ADC1_EXP_SEL1	SPI3_SOUT	SPI1_SCK		TMU_OUT9								JTAG_TDO_ SWD_SWO
165	137	93	PTE_1		PTE_1	SPI0_SIN	ADC1_EXP_SEL0	I2C1_SCL	SPI1_PCS0	eTMR1_FLT1	TMU_OUT10		SPI0_SCK		UART7_TX			MPWM1_CH10	
166	138	94	PTE_0	ADC0_S_EXP	PTE_0	SPI0_SCK	TCLK_IN1	I2C1_SDA	SPI1_SOUT	eTMR1_FLT2	TMU_OUT11		SPI0_SIN		UART7_RX			MPWM1_CH11	
167			PTE_26		PTE_26	eTMR3_CH6	MPWM0_CH6											MPWM1_CH12	
168	139	95	PTC_5		PTC_5	eTMR2_CH0	RTC_CLKOUT	SPI3_PCS1		eTMR2_QD_PHB			SPI1_SIN					MPWM1_CH13	JTAG_TDI
169	140	96	PTC_4	ACMP0_IN2	PTC_4	eTMR1_CH0	RTC_CLKOUT			eTMR1_QD_PHB			EWDG_IN						JTAG_TCK_ SWD_CLK
170	141	97	PTA_5		PTA_5	CAN3_TX	TCLK_IN1												RCU_RESET_b
171			VSS	VSS															
172			VDD	VDD															
173	142	98	PTA_4		PTA_4	CAN3_RX		ACMP0_OUT	EWDG_OUT_b										JTAG_TMS_ SWD_IO
174			PTE_27		PTE_27	eTMR3_CH7	MPWM0_CH7												
175	143	99	PTA_9	ADC0_S31	PTA_9	UART2_TX	SPI2_PCS0	SPI1_SIN	eTMR3_FLT2	eTMR1_FLT3			SPI3_PCS0					MPWM1_CH14	
176	144	100	PTA_8	ADC0_S26	PTA_8	UART2_RX	SPI2_SOUT	SPI1_SCK	eTMR3_FLT3				MPWM0_CH4					MPWM1_CH15	

7.2 Packages

The information of package pinouts is as follows:

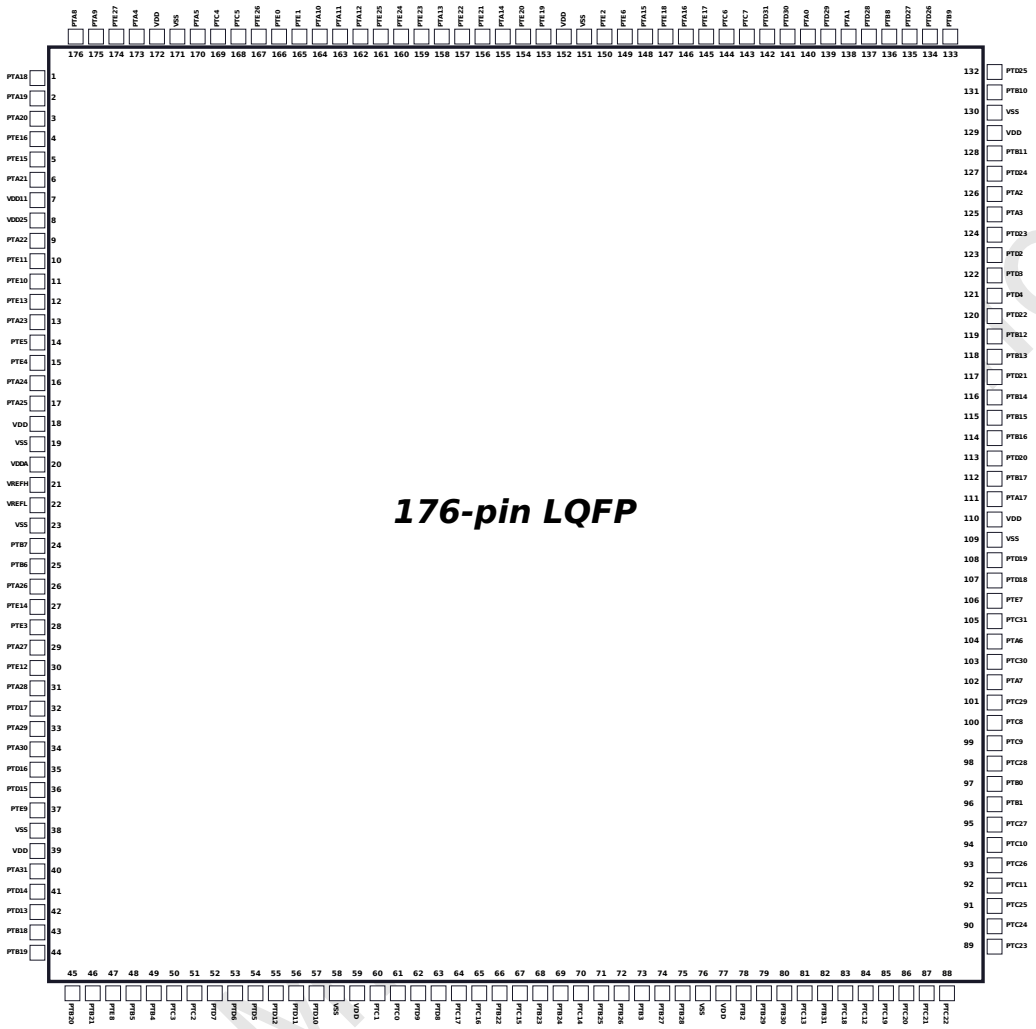


Figure 13: 176-pin LQFP Package

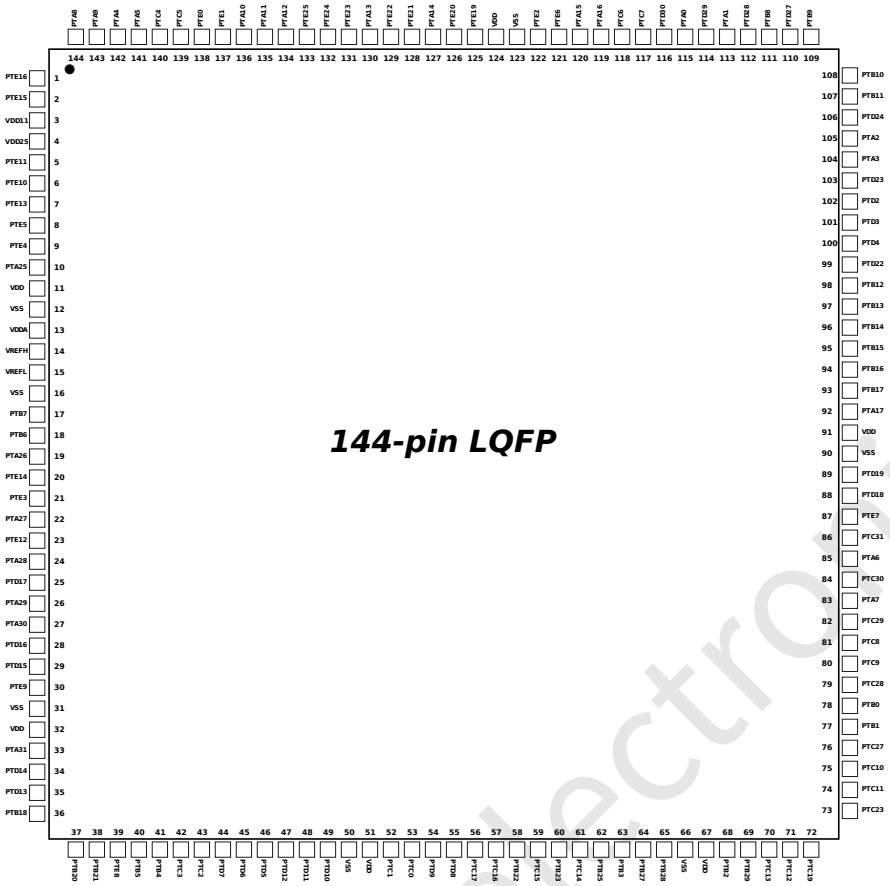


Figure 14: 144-pin LQFP Package

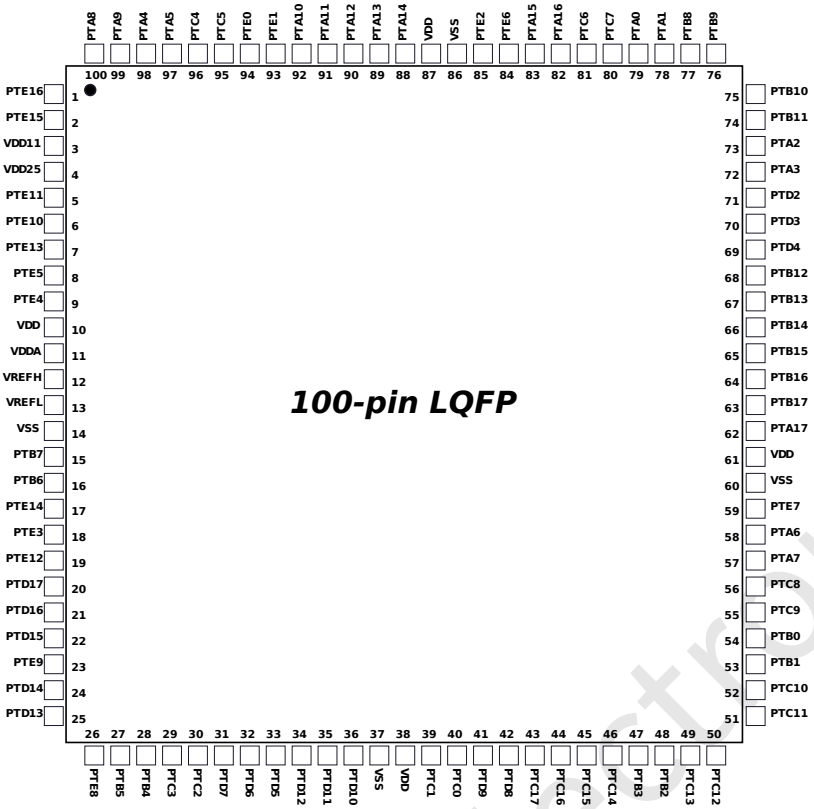
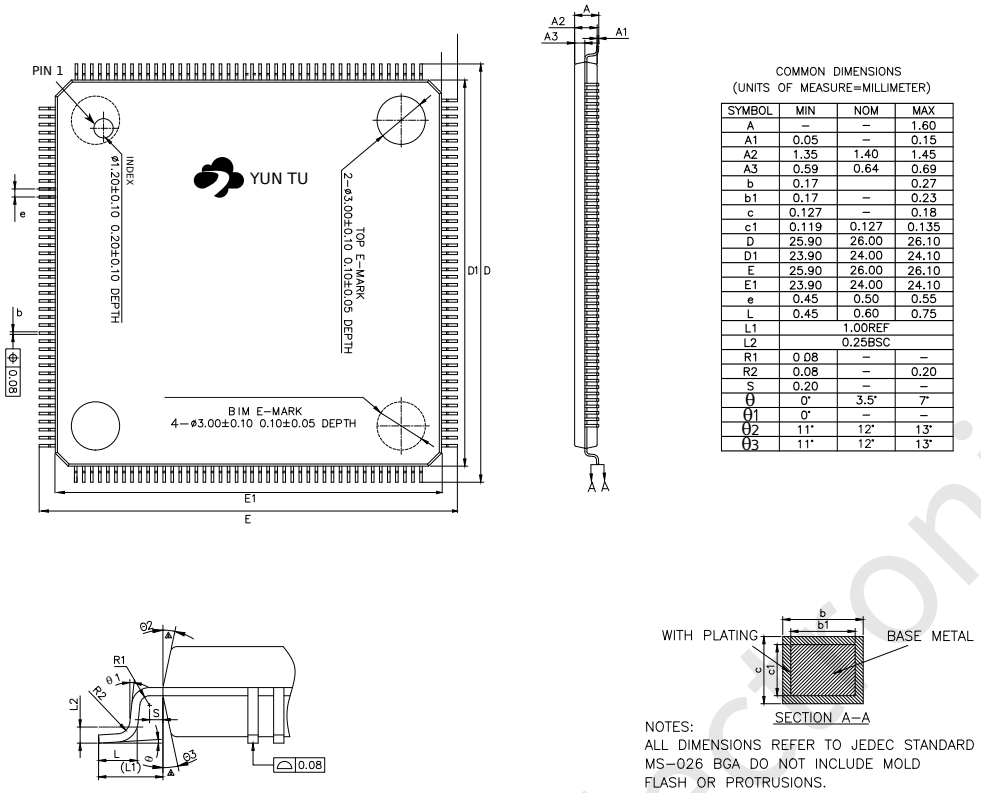


Figure 15: 100-pin LQFP Package

Note: The chip mark will not contain packing information(T/R)

7.3 Dimensions

Package dimensions are as follows:

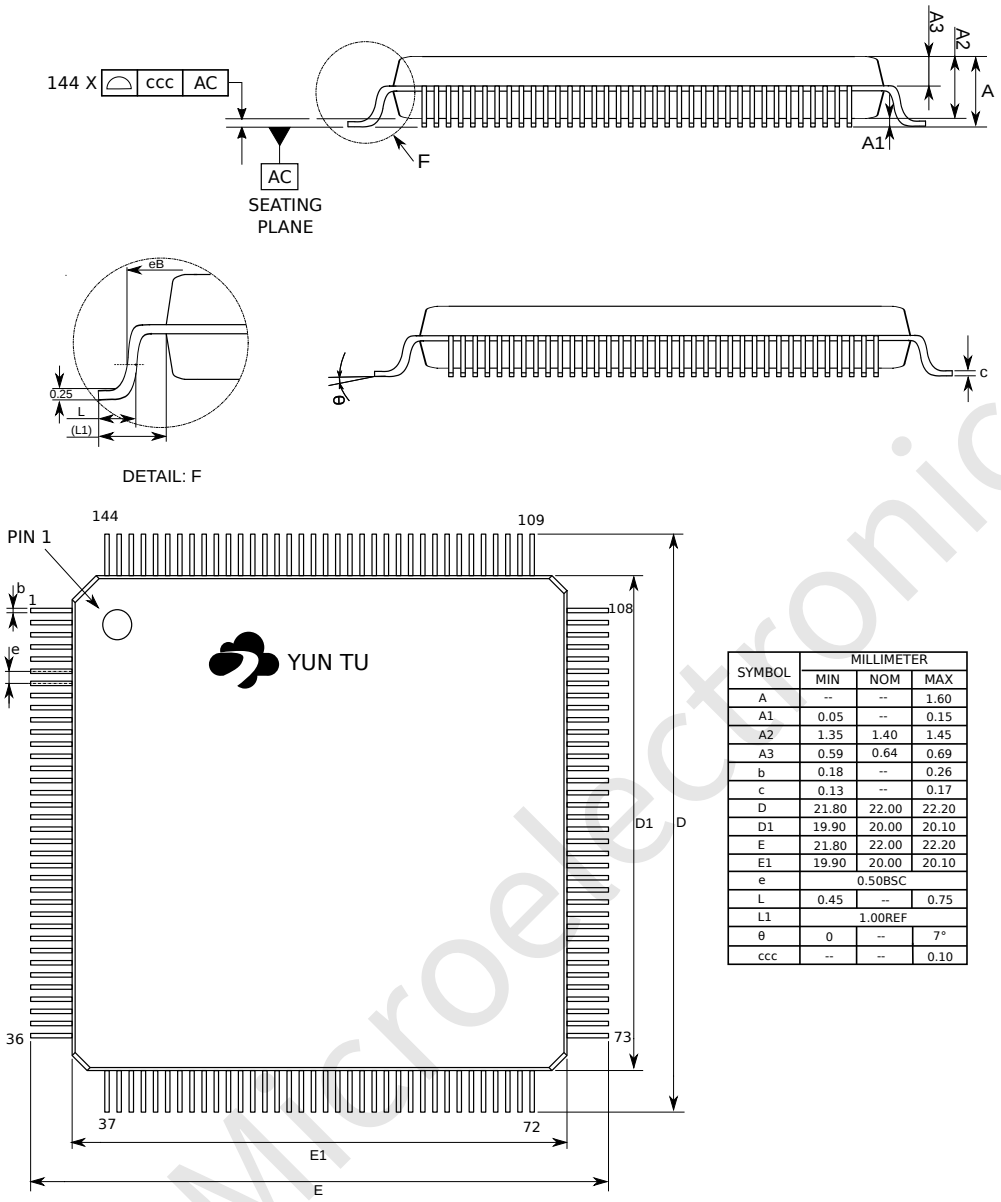


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17		0.27
b1	0.17	–	0.23
c	0.127	–	0.18
c1	0.119	0.127	0.135
D	25.90	26.00	26.10
D1	23.90	24.00	24.10
E	25.90	26.00	26.10
E1	23.90	24.00	24.10
e	0.45	0.50	0.55
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

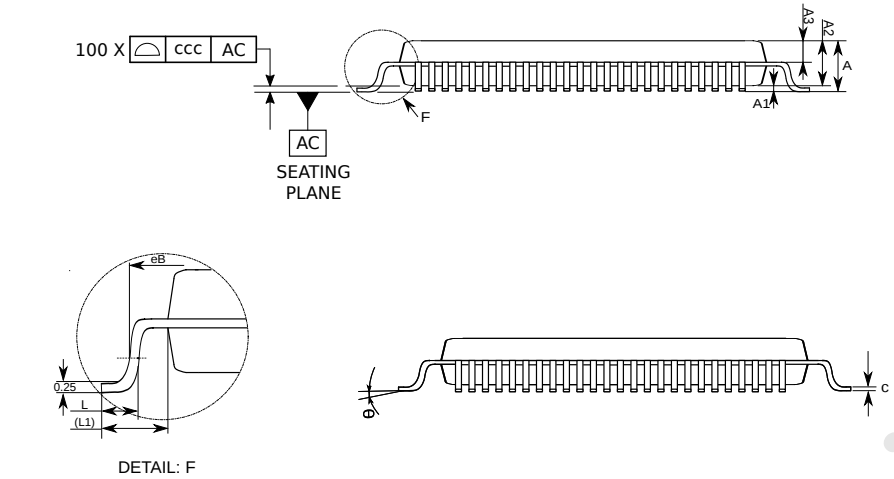
NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BGA DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 16: 176pin LQFP



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
c	0.13	--	0.17
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°
ccc	--	--	0.10

Figure 17: 144pin LQFP



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
c	0.13	--	0.17
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
eB	15.05	--	15.35
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°
ccc	--	--	0.08

Figure 18: 100pin LQFP

Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2024/2/2	Initial version

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