YTM32B1LD0x Data Sheet

Support: YTM32B1LD04H0VLHT, YTM32B1LD04H0VLFT, YTM32B1LD04H0VLET

Document Number: YTM32B1LD0x DS

Rev.1.7, 2023/7/21

1 Features Summary

- AEC-Q100 qualified
- ARM Cortex-M0+
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Single-cycle access to I/O: Up to 50 percent faster than standard I/O, improves reaction time to external events allowing bit manipulation and software protocol emulation
  - Two-stage pipeline: Reduced number of cycles per instruction (CPI), enabling faster branch instruction and ISR entry, and reducing power consumption
  - Excellent code density in comparison to 8-bit and 16-bit MCUs: Reduced flash size, system cost and power consumption
  - 100 percent compatible with ARM Cortex-M0 and a subset ARM Cortex-M3/M4: Reuse existing compilers and debug tools
  - Simplified architecture: 56 instructions and 17 registers enable easy programming and efficient packaging of 8/16/32-bit data in memory
  - Linear 4 GB address space removes the need for paging/banking, reducing software complexity
  - ARM third-party ecosystem support: Software and tools to help minimize development time/cost
  - Support systick with a 8-bit divider and enablement
- 16 DMA channels with 64 hardware trigger sources
- DIVSQRT module with 32-bit integer divide and square root arithmetic operations
- Memory
  - Up to 64 KB Program Flash (PFlash) with ECC
  - Up to 8 KB SRAM with ECC
  - Single power supply (2.7 ~ 5.5 V) with full functional flash program/erase/read operations
- Clocks
  - 8~24 MHz External Oscillator (EOSC)
  - Up to 48 MHz Fast Internal RC Oscillator (FIRC)
  - 128 KHz Slow Internal RC Oscillator (SIRC) for system
  - 2 KHz Slow Internal RC Oscillator (SIRC) for RTC
- Power Management
  - Low-power ARM Cortex-M0+ with excellent energy efficiency
  - Support four power modes: Active, Sleep, Deepsleep and Standby
  - Support clock gating for unused modules
  - Support specific peripherals remain working in low power modes
- Mixed-signal Analog
  - Support one Analog-to-Digital Converter (ADC) with up to 16 external single end channels, and sample rate is 1Msps
  - Support one Analog Comparator (ACMP) with 8 channels
- Communications
  - Up to three Universal Asynchronous Receiver Transmitter (UART) with optional 13-bit break, full duplex Non-return to Zero (NRZ) and LIN extension support
  - Up to three Serial Port Interface (SPI) with full-duplex or single-wire bidirectional and master or slave mode
  - Up to two Inter-integrated Circuit (I2C)
  - One FlexCAN support CAN2.0A/B and FD
- Reliability, Safety and Security
  - Clock Monitor Unit (CMU)
  - Internal Watchdog (WDG) with independent clock source
  - Cyclic Redundancy Check (CRC) with programmable 16-bit or 32-bit polynomial generator
- Timers
  - Up to three Enhanced Timers (eTMR)
  - Periodic Timer (pTMR) for RTOS task scheduler time base for timer modules
  - Low Power Timer (lpTMR)
  - 16-bit Real Time Clock (RTC)
- Human-Machine Interface
  - Up to 57 GPIO pins with interrupt functionality
  - Non-Maskable Interrupt (NMI)
- Operating Characteristics
  - Voltage range: 2.7V ~ 5.5V
  - Ambient temperature range: -40°C ~ 105°C
  - Junction temperature range: -40°C ~ 125°C
- I/O and package
  - Support LQFP 64/48/32

Contents

2 Overview

YTM32B1LD0x series provide the highly scalable portfolio of ARM® Cortex®-M0+ MCUs in the automotive industry. With 2.7 ~ 5.5 V supply and focus on exceptional EMC/ESD robustness, YTM32B1LD0x series devices are well suited to a wide range of applications in electrical harsh environments, and is optimized for cost-sensitive applications offering low pin count option. The YTM32B1LD0x series offers a broad range of memory, peripherals and package options. They share common peripherals and pin counts allowing developers to migrate easily within an MCU family or among the MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the YTM32B1LD0x series for their end product platforms, maximizing hardware and software reuse and reducing time-to-market.

3 Block Diagram

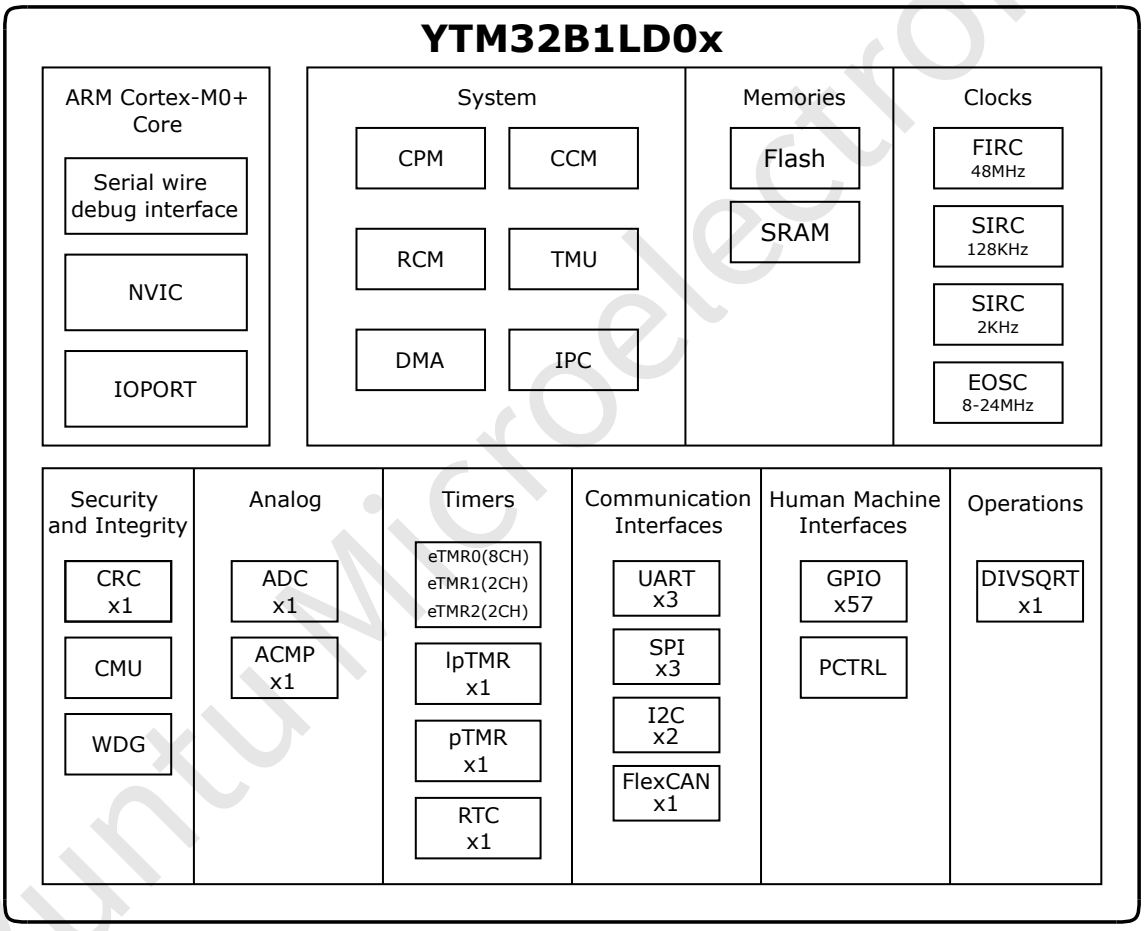


Figure 1: YTM32B1LD0x Block Diagram

4 Features

The following sections describe the high-level module features for YTM32B1LD0x device.

4.1 Core Modules

4.1.1 ARM Cortex-M0+

- Up to 48 MHz core frequency from 2.7 V to 5.5 V
- Support up to 32 interrupt request sources
- 2 stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial wire debug (SWD) reduces the number of pins required for debugging
- Single cycle 32 bits by 32 bits multiplier

4.1.2 Nested Vector Interrupt Controller (NVIC)

- Up to 32 interrupt sources
- Support four priority levels for interrupts with two bits in each IPRn registers
- Includes a single non-maskable interrupt

4.1.3 Debug Controller

- 2-pin serial wire debug (SWD) provides external debugger interface

4.2 System Modules

4.2.1 Clock and Power Control Modules (CPM)

- Four system clock sources
  - Internal high speed 48 MHz oscillator
  - Internal low speed 128 KHz oscillator
  - External high speed 8~24MHz crystal/resonator
  - Power control clock (PwrCtrlClk)
- Individual clock divider for System and Bus clock
- Support multiple low voltage detection
- Support BOR (Brown Out Reset)
- Support multiple low power modes

4.2.2 IP Controller (IPC)

- Peripheral Bus clock enable
- IPC clock source selection as follows:
  - Bus clock
  - Fast Internal RC Oscillator (FIRC) 48 MHz
  - External Oscillator (EOSC) 8~24 MHz
  - Slow Internal RC Oscillator (SIRC) 128 KHz
- IPC clock divide values from 1 to 16

4.2.3 Reset Controller Module (RCM)

- Eight sources of reset:
  - Power on reset and Brown Out reset
  - Force power on reset

  - CPU lockup reset
  - External reset pin
  - Software reset
  - Watchdog timer reset
  - Clock monitor reset
  - Deepsleep acknowledge timeout reset
- Software-readable status flags indicating the cause of the last reset

4.2.4 Chip Configuration Module(CCM)

- Configure wakeup functions
- Configure Digital Glitch Filter of RESET_b pin

4.2.5 Trigger Multiplex Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources

4.2.6 Direct Memory Access (DMA)

- All address range data transfer from source to destination
- Support separate source/destination data size configuration
  - Word(32-bit), half word(16-bit), byte(8-bit) transfer size
- Support separate source/destination address offset configuration
  - Address increase/decrease/not change selectable
- Up to 16 DMA channels
  - Fix priority and round-robin arbitration
  - Support channel to channel link
- Software/Hardware/Link trigger
- Up to 64 peripheral hardware triggers
- Internal data fifo for data transfer
- Support update DMA transfer information from system memory after transfer complete
- Support data transfer loop and trigger loop

4.3 Memories

4.3.1 Embedded Flash Module (EFM)

- 64 KB Program Flash (PFlash) with ECC which supports single error correction (SEC) and double error detection (DED)
- 2 KB Data Flash (DFlash) with ECC support
- 24 MHz single cycle reads of bytes, aligned halfword (16-bit) and aligned word (32-bit)
- Automated generation of ECC parity while programming and erasing
- Optional interrupt on command completion
- Program and erase operations do not require any special power sources other than the normal VDD supply

4.3.2 On-chip SRAM

- 8 KB SRAM with ECC supports single error correction (SEC) and double error detection (DED)

4.4 Analog

4.4.1 Analog-to-Digital Converter (ADC)

- Support 12-bit, 10-bit, 8-bit and 6-bit single-ended configurable resolution
- Up to 1.0μs for 12-bit resolution conversion time
- Support DMA and conversion result FIFO with watermark
- Support 15 analog channels measure
- Support multiple conversion mode
  - Support conversion for a single channel or scan a sequence of channels
  - Single conversion mode to convert selected inputs once a trigger
  - Continuous mode to convert selected inputs continuously
  - Discontinuous mode
- Support analog watchdog
- Interrupt generation at the end of sampling, the end of conversion, the end of sequence conversion, and in case of analog watchdog or overrun events

4.4.2 Analog Comparator (ACMP)

- Up to 8 channels
- Operational over the entire supply range
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge or both edges of the comparator output
- Selectable inversion on comparator output
- Digitally filtered, Filter can be bypassed
- Two software selectable performance levels
  - Shorter propagation delay at the expense of higher power
  - Low power with longer propagation delay
- A comparison event can be selected to trigger DMA transfer
- Functional in Deepsleep mode available
- Up to 4 channels can be used to execute automatic scan comparisons
- Comparison ways in continuous mode: one-shot mode and loop mode

4.5 Timer

4.5.1 Periodic Timer (pTMR)

- Timers can generate interrupts
- Four channels of 32-bit timers, each timer has independent timeout periods
- Ability to stop in debug mode
- Support chain mode to connect multiple timer to a longer timer

4.5.2 Low Power Timer (lpTMR)

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wake-up from any low power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler and glitch filter

- Configurable input source for pulse counter
  - Rising-edge
  - Falling-edge
- Support triggering DMA transfer

4.5.3 Enhanced Timer (eTMR)

- There are three eTMRs with below configurations
  - eTMR0: 8 channels
  - eTMR1: 2 channels
  - eTMR2: 2 channels
- Input clock and external clock can be the source clock of each eTMR
- Each eTMR contains a clock prescaler divided by 1, 2, 4, 8, 16, 32, 64 or 128
- Each eTMR contains a 16-bit counter
- Each channel can be configured as three modes as follow
  - Input Capture mode
    - Support rising edges, falling edges or dual edges
    - An input filter with a prescaler can be selected for channel 0 ~ 3 of eTMR0
  - Output Compare mode
    - The output signal can be configured to set, clear or toggle on match point
  - PWM mode
    - Edge-aligned PWM mode for each channel
    - Center-aligned PWM mode for each channel
    - Each complementary PWM mode for pair channels supports deadtime insertion
- Each eTMR can be configured to generate triggers on match point
- PWM outputs can be controlled by software
- Polarity control is available for every channel of each eTMR
- Synchronized loading of shadow registers is available in each eTMR
- eTMR0 supports 4 fault inputs for global fault control
- Only eTMR0 supports fault interrupt
- The channel interrupt is available in each eTMR
- The counter overflow interrupt is available in each eTMR

4.5.4 Real Time Clock (RTC)

- 32-bit seconds counter with overflow flag and optional interrupt
- Configurable 32-bit alarm
- 16-bit prescaler with compensation that can correct errors
- Option to increment prescaler using a 1 kHz Clock (prescaler increments by 32 every clock edge)
- Register write protection
- Configurable 1, 2, 4, 8, 16, 32, 64 or 128 Hz square wave output with optional interrupt
- Lock support of register access for control and alarm register
- Support two clock sources
  - 32 KHz (128 KHz SIRC div4)
  - 1 KHz (2 KHz SIRC div2)

4.6 Security, Integrity and Safety

4.6.1 Cyclic Redundancy Check (CRC)

- The following CRC polynomials are implemented:
  - CRC16 (CRC-CCITT):
    $X^{16} + X^{12} + X^5 + 1$
  - CRC32 (CRC-ethernet):
    $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable initial seed
- Optional bit-swap in one byte is available for input data
- Optional bit-swap in one word is available for output data
- Optional bit-inversion is available for output data
- 8/16/32-bit access for CRC input data

4.6.2 Watchdog (WDG)

- 32-bit countdown timer
- Support regular or window servicing mode
- Support reset request or interrupt for the first timeout
- Hard and soft configuration lock bits
- Support fixed key for dog feeding

4.6.3 Clock Monitor Unit (CMU)

- Support two clock monitors: CMU0 and CMU1. CMU0 is used for monitor master clock. CMU1 is used for monitor bus clock.
- Support check three type errors: checked clk loss, reference clk loss, checked clk out of range.
- Support reset generation based on CMUs' errors.
- support selectable reference clk between FIRC and EOSC, and could set to select a moderate reference clk frequency.
- Each CMU has its own configuration: enable, reset enable, checked clk expected range, and reference clk divider.

4.7 Operation Unit

4.7.1 Divide and Square Root (DIVSQRT)

- Lightweight implementation of 32-bit integer divide and square root arithmetic operations.
  - Supports 32/32 signed and unsigned divide (or remainder) calculation
  - Supports 32-bit unsigned square root calculation
- Simple programming model includes registers of input data, result, control, status.
- Programming model interface optimized for activation from inline code or software library call.
  - "Fast Start" configuration minimizes the memory-mapped register write overhead.
  - Supports two methods to determine when the result is valid, including software polling.
  - Configurable divide-by-zero response
- Pipelined design process 2bits per cycle with early termination exit for minimum execution time.

4.8 Communication Interfaces

4.8.1 Flexible Controller Area Network (FlexCAN)

- Full implementation of the CAN FD protocol and CAN Specification 2.0 Part B

  - Standard data frames
  - Extended data frames
  - Zero to sixty-four bytes data length
  - Programmable bit rate
  - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Silicon-proven implementation passing ISO 16845-1:2016 CAN conformance tests
- Flexible mailboxes configurable to store 0 to 8, 16, 32 or 64 bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Rx FIFO with storage capacity for up to six frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Flexible message buffers, totaling 32 message buffers of 8 bytes data length each, configurable as Rx or Tx
- Programmable clock source to the CAN Protocol Engine, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low-power modes, with programmable wake-up on bus activity
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the FlexCAN is synchronous with CAN bus
- CRC status for transmitted message
- Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard or 512 partial (8-bit) IDs, with up to 32 ID Filter Table elements
- Supports detection and correction of errors in memory read accesses. Each byte of FlexCAN memory is associated to 5 parity bits. The error correction mechanism ensures that in this 13-bit word, errors in one bit can be corrected (correctable errors) and errors in 2 bits can be detected but not corrected (non-correctable errors).

4.8.2 Universal Asynchronous Receiver/Transmitter (UART)

- Support LIN mode
- Transmit/Receive FIFO
- Support Transmit/Receive via DMA
- Baud rate setting
- 1-bit or 2-bit STOP size
- 7-bit, 8-bit, 9-bit or 10-bit frame size
- Transmit/Receive polarity setting

- Receive data match
- Line idle, address match wake-up
- Support transmit/receive line switch

4.8.3 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration
- Configurable frame size
- Transmit/Receive FIFO
- Support single line mode
- Support Master and slave mode
- Support Transmit/Receive via DMA

4.8.4 Inter-Integrated Circuit (I2C)

- Support standard, fast and ultra fast mode
- Support 7-bit/10-bit address mode with master and slave
- Support SMBUS mode
- Support multi-master arbitration and synchronization
- Support Master and slave clock stretching
- Transmit/Receive FIFO (Master only)
- Analog and digital filter on both SCL and SDA pins
- Support Transmit/Receive via DMA

4.9 Human Machine Interface

4.9.1 General Purpose Input/Output (GPIO)

- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- Digital filter for data inputs
- Inversion for data inputs
- Interrupt flag and enable registers for each pin
- Support for edge sensitive (rising, falling, both) or level sensitive (low, high)
- Asynchronous wake-up in low-power modes
- Pin interrupt is functional in all digital pin muxing modes

4.9.2 Port Controller (PCTRL)

- Individual pull control fields with pullup, pulldown, and pull-disable support
- Individual slew rate field supporting fast and slow slew rates
- Individual input passive filter field supporting enable and disable of the individual input passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to 6 chip-specific digital functions

5 Ordering Information

The following chips are available for ordering.

Table 1: Ordering Information

Product	Memory		Package		IO and ADC channel		Communication
Part number	Flash(KB)	SRAM(KB)	Pin count	Package	GPIOs (Normal)	ADC channels	FlexCAN
YTM32B1LD04H0VLHT	64KB	8KB	64	LQFP	57	16	1
YTM32B1LD03H0VLHT	32KB	4KB	64	LQFP	57	16	1
YTM32B1LD02H0VLHT	16KB	2KB	64	LQFP	57	16	1
YTM32B1LD01H0VLHT	8KB	1KB	64	LQFP	57	16	1
YTM32B1LD04H0VLFT	64KB	8KB	48	LQFP	42	14	1
YTM32B1LD03H0VLFT	32KB	4KB	48	LQFP	42	14	1
YTM32B1LD02H0VLFT	16KB	2KB	48	LQFP	42	14	1
YTM32B1LD01H0VLFT	8KB	1KB	48	LQFP	42	14	1
YTM32B1LD04H0VLET	64KB	8KB	32	LQFP	27	13	1
YTM32B1LD03H0VLET	32KB	4KB	32	LQFP	27	13	1
YTM32B1LD02H0VLET	16KB	2KB	32	LQFP	27	13	1
YTM32B1LD01H0VLET	8KB	1KB	32	LQFP	27	13	1

5.1 Part Numbers

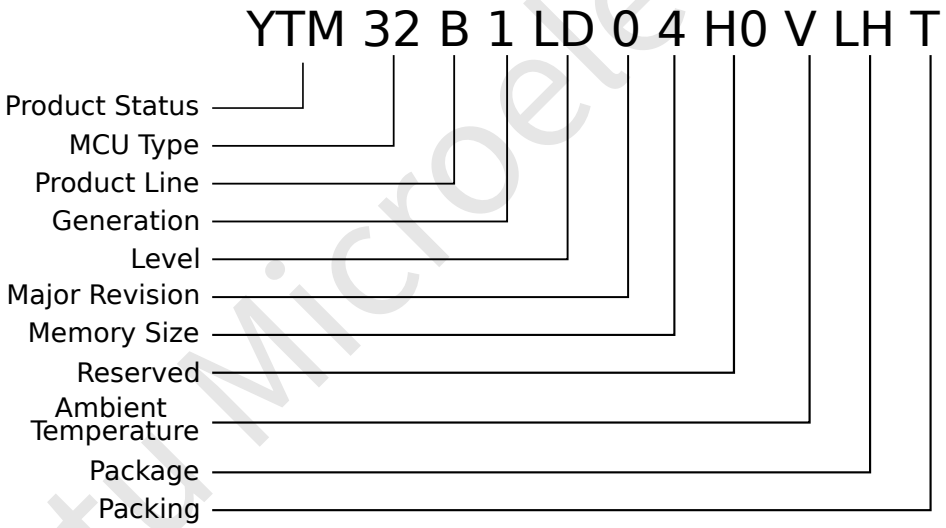


Figure 2: Part Numbers Field

The part numbers field description is shown as below.

Table 2: Part Number Field Description

Field	Description	Values
YTM	Product Status	YTM: Qualified PTM: Prototype
32	MCU Type	32: 32-bit

Table 2: Part Number Field Description

Field	Description	Values					
B	Product Line	B: General D: Dashboard P: Powertrain V: Vision N: Network					
1	Generation	1st generation product					
Lx	Level	Hx: High end Mx: Middle end Lx: Low end					
0	Major Revision	1st revision					
4	Memory Size		1	2	3	4	5
		H	2M	4M	6M	8M	-
		M	64K	128K	256K	512K	1M
		L	8K	16K	32K	64K	128K
H0	Reserved	Reserved					
V	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C					
LH	Package	Pin Counts	LQFP	QFN	BGA	-	-
		32	LE	FM	-	-	-
		48	LF	-	-	-	-
		64	LH	-	-	-	-
		100	LL	-	MH	-	-
		144	LQ	-	-	-	-
		176	LU	-	-	-	-
		257	-	-	MM	-	-
		289	-	-	MQ	-	-
T[1]	Packing	T: Trays/Tubes R: Tape and Reel					

1. The chip mark will not contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Patameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ C-Grade\ Part}$	Ambient temperature under bias	-40	–	85	°C
$T_{J\ C-Grade\ Part}$	Junction temperature under bias	-40	–	105	°C
$T_{A\ V-Grade\ Part}$	Ambient temperature under bias	-40	–	105	°C
$T_{J\ V-Grade\ Part}$	Junction temperature under bias	-40	–	125	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	-500	500	V	
	Corner pins only	-1500	1500	V	
I_{LAT}	Latch-up current at ambient temperature of 105 °C	-50	50	mA	3
	Latch-up current at ambient temperature of 25 °C	-200	200	mA	

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

6.2 DC Characteristics

6.2.1 Absolute Maximum Ratings

Table 6: Absolute maximum ratings for YTM32B1LD0x series

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	-0.3	5.8	V	
I_{VDD}	Maximum current into V_{DD}	–	120	mA	

Table 6 continued from previous page

Symbol	Description	Min.	Max.	Unit	Notes
V_{IO}	Digital/Analog IO Input voltage	-0.3	V_{DD} + 0.3	V	
I_O	Instantaneous maximum current of single pin	-25	25	mA	
V_{DDA}	Analog supply voltage	V_{DD} - 0.3	V_{DD} + 0.3	V	

NOTE:

- The maximum ratings are the limits to which the device can be subjected without permanently damaging the device.
- The device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2.2 Voltage and Current Operating Requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	5.5	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	
$V_{DD} - V_{DDA}$	V_{DD} to V_{DDA} differential voltage	-0.1	0.1	V	
I_{ICIO}	DC injection current - single pin				
	$V_{IN} < V_{SS}$ - 0.3V (Negative current injection)	-3	–	mA	1
	$V_{IN} < V_{SS}$ + 0.3V (Negative current injection)	–	3	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive rejection currents of 16 contiguous pins	-25	25	mA	

1. All pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{SS} – 0.3V or greater than V_{DD} + 0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{SS}–0.3V–V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R = [V_{IN}–(V_{DD} + 0.3V)]/|I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.

6.2.3 DC Electrical Specifications at 3.3V

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	2.7	3.3	4.0	V	
V_{ih}	Input buffer high voltage	0.7 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.3 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	4.8	–	mA	

Table 8 continued from previous page

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	–	7.3	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin)	–	50	–	nA	
V_{OH}	Output high voltage					
	Normal drive pad ($2.7V \leq V_{DD} \leq 4.0V$, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	–	V	
V_{OL}	Output low voltage					
	Normal drive pad ($2.7V \leq V_{DD} \leq 4.0V$, I_{OL} = -2.8mA)	–	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	–	0.002	–	μA	
R_{PU}	Internal pull-up resistors	20	–	100	kΩ	
R_{PD}	Internal pull-down resistors	20	–	105	kΩ	

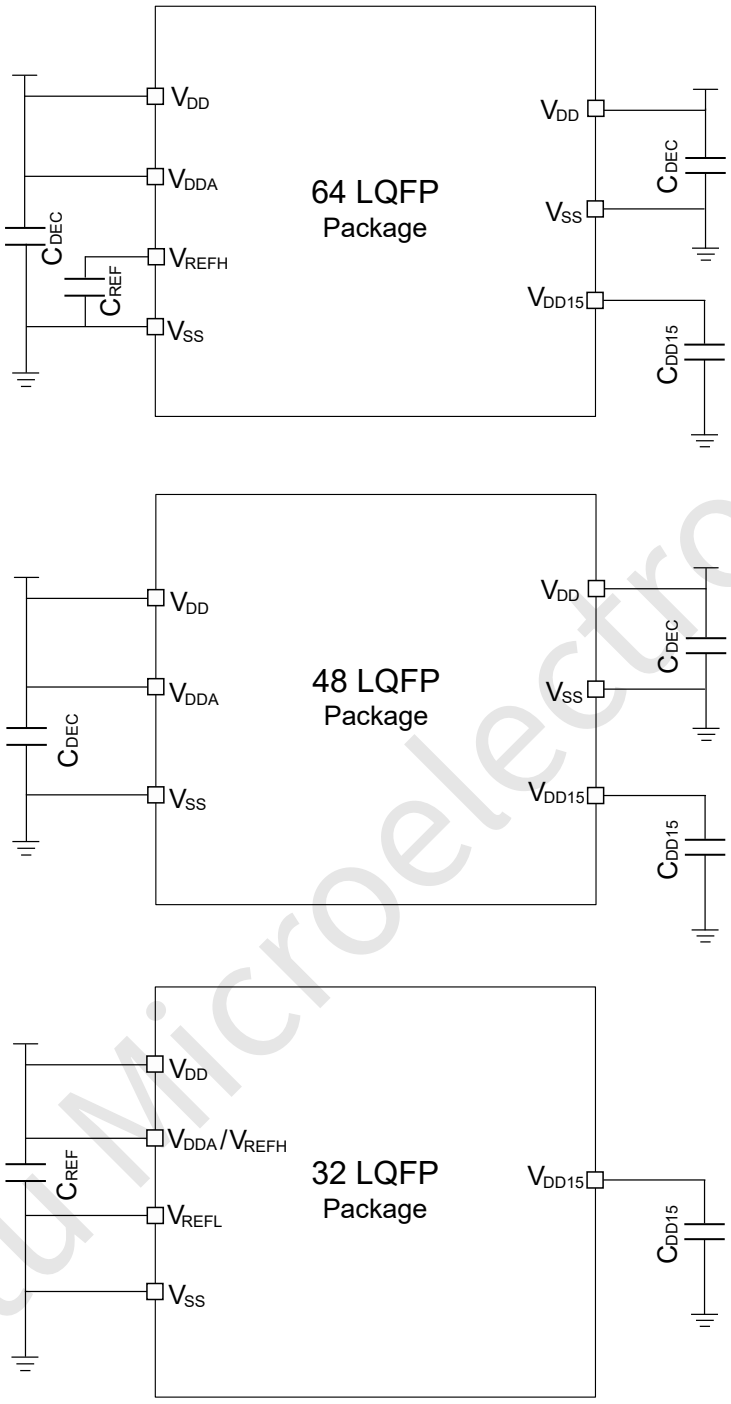
6.2.4 DC Electrical Specifications at 5.0V

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	4	5	5.5	V	
V_{ih}	Input buffer high voltage	0.65 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.35 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	6	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	–	8.6	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin)	–	380	–	nA	
V_{OH}	Output high voltage					
	Normal drive pad ($2.7V \leq V_{DD} \leq 4.0V$, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	–	V	
V_{OL}	Output low voltage					
	Normal drive pad ($2.7V \leq V_{DD} \leq 4.0V$, I_{OL} = -2.8mA)	–	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	100	mA	

Table 9 continued from previous page

Symbol	Patameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	–	0.005	0.5	μA	
R_{PU}	Internal pull-up resistors	20	–	70	kΩ	
R_{PD}	Internal pull-down resistors	20	–	70	kΩ	

6.2.5 Voltage Regulator Electrical Characteristics



NOTE: V_{DD} and V_{DDA} must be shorted to a common source on PCB design

Figure 3: Pinout decoupling

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF}[1,2]	ADC reference high decoupling capacitance	–	100	–	nF
C_{DEC}[2,3]	Recommended decoupling capacitance	–	100	–	nF
C_{DD15}[4]	Internal PMC, LDO voltage	–	1	–	μF

1. For improved ADC performance it is recommended to use 1 nF X7R/C0G and 10 nF X7R ceramics in parallel.
2. The capacitors should be placed as close as possible to the VREFH/VREFL pins or corresponding VDD/VSS pins.
3. The requirement and value of of CDEC will be decided by the device application requirement.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB design.

6.2.6 POR, LVR and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	–	2.5	–	V	
V_{LVD}	Falling low-voltage threshold(LVDCFG=0)	–	1.9	–	V	
	Falling low-voltage threshold(LVDCFG=1)	–	2.15	–	V	
	Falling low-voltage threshold(LVDCFG=2)	–	2.41	–	V	
	Falling low-voltage threshold(LVDCFG=3)	–	2.68	–	V	
	Falling low-voltage threshold(LVDCFG=4)	–	2.94	–	V	
	Falling low-voltage threshold(LVDCFG=5)	–	3.21	–	V	
	Falling low-voltage threshold(LVDCFG=6)	–	3.48	–	V	
	Falling low-voltage threshold(LVDCFG=7)	–	3.75	–	V	
	Falling low-voltage threshold(LVDCFG=8)	–	4.02	–	V	
	Falling low-voltage threshold(LVDCFG=9)	–	4.27	–	V	
	Falling low-voltage threshold(LVDCFG=10)	–	4.47	–	V	
	Falling low-voltage threshold(LVDCFG=11)	–	4.65	–	V	
	Falling low-voltage threshold(LVDCFG=12)	–	4.85	–	V	
	Falling low-voltage threshold(LVDCFG=13)	–	5.04	–	V	
V_{LVD_HYST}	LVD hysteresis(LVD5VHYS=01b)	-2	–	2	%	
	LVD hysteresis(LVD5VHYS=10b)	-4.2	–	4.2	%	
	LVD hysteresis(LVD5VHYS=11b)	-8.4	–	8.4	%	

6.2.7 Power Mode Transition Operating Behaviors

Description	System clock	Core, bus frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	FIRC	48MHz, 24MHz	–	1.5μs	–
SLEEP -> ACTIVE	EOSC	24MHz, 12MHz	–	5μs	–
DEEPSLEEP -> ACTIVE	FIRC	48MHz, 24MHz	–	50μs	–
DEEPSLEEP -> ACTIVE	EOSC	24MHz, 12MHz	–	10μs	–
STANDBY -> ACTIVE	FIRC	48MHz, 24MHz	–	50μs	–
STANDBY -> ACTIVE	EOSC	24MHz, 12MHz	–	10μs	–
T_{POR}	FIRC(reset value)	48MHz, 24MHz	–	2.8ms	–

6.2.8 Power Consumption

Mode	Symbol	Clock configuration	Description	Temperature	Min	Typ	Max	Units
Active	I_{DD_ACTIVE}	FIRC	Running coremark in flash, all peripheral clock enabled. core @48MHz, bus @24MHz V_{DD}=5V	25 °C	–	15.9	–	mA
				105 °C	–	–	–	mA
			Running coremark in flash, all peripheral clock disabled. core @48MHz, bus @24MHz V_{DD}=5V	25 °C	–	10.8	–	mA
				105 °C	–	–	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @48MHz, bus @24MHz V_{DD}=5V	25 °C	–	15.7	–	mA
				105 °C	–	–	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @48MHz, bus @24MHz V_{DD}=5V	25 °C	–	10.8	–	mA
				105 °C	–	–	–	mA
		EOSC	Running coremark in flash, all peripheral clock enabled. core @48MHz, bus @24MHz V_{DD}=5V	25 °C	–	11.5	–	mA
				105 °C	–	–	–	mA
			Running coremark in flash, all peripheral clock disabled. core @48MHz, bus @24MHz V_{DD}=5V	25 °C	–	9.0	–	mA
				105 °C	–	–	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @48MHz, bus @24MHz V_{DD}=5V	25 °C	–	15.7	–	mA
				105 °C	–	–	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @48MHz, bus @24MHz V_{DD}=5V	25 °C	–	10.8	–	mA
				105 °C	–	–	–	mA
SLEEP	I_{DD_SLEEP}	–	Sleep mode current, V_{DD}=5V	≤ 25 °C	–	7.2	–	mA
				105 °C	–	–	–	mA
DEEPSLEEP	$I_{DD\_DEEPSLEEP}$	FIRC	Deepsleep mode current, V_{DD}=5V PMCLPEN=0, FLSLPEN=1, BOREN=0, LVDLPMD=0, LVDEN=0	≤ 25 °C	–	51.3	–	μA
				105 °C	–	–	–	mA
			Deepsleep mode current, V_{DD}=5V PMCLPEN=0, FLSLPEN=1, BOREN=1, LVDLPMD=0, LVDEN=0	≤ 25 °C	–	53.2	–	μA
				105 °C	–	–	–	mA
			Deepsleep mode current, V_{DD}=5V PMCLPEN=0, FLSLPEN=1, BOREN=1, LVDLPMD=0, LVDEN=1	≤ 25 °C	–	54.4	–	μA
				105 °C	–	–	–	mA
			Deepsleep mode current, V_{DD}=5V PMCLPEN=0, FLSLPEN=1, BOREN=1, LVDLPMD=1, LVDEN=1	≤ 25 °C	–	53.3	–	μA
				105 °C	–	–	–	mA
STANDBY	$I_{DD\_STANDBY}$	FIRC	Standby mode current, V_{DD}=5V PMCLPEN=1, FLSLPEN=1, BOREN=0, LVDLPMD=0, LVDEN=0	≤ 25 °C	–	0.6	–	μA
				105 °C	–	–	–	mA
			Standby mode current, V_{DD}=5V PMCLPEN=1, FLSLPEN=1, BOREN=1, LVDLPMD=0, LVDEN=0	≤ 25 °C	–	2.6	–	μA
				105 °C	–	–	–	mA
			Standby mode current, V_{DD}=5V PMCLPEN=1, FLSLPEN=1, BOREN=1, LVDLPMD=0, LVDEN=1	≤ 25 °C	–	3.8	–	μA
				105 °C	–	–	–	mA
			Standby mode current, V_{DD}=5V PMCLPEN=1, FLSLPEN=1, BOREN=1, LVDLPMD=1, LVDEN=1	≤ 25 °C	–	2.6	–	μA
				105 °C	–	–	–	mA

6.2.9 Power Sequence

6.2.9.1 Power Up Sequence

Hardwares must follow sequence below to ensure that the chip is powered up properly.

1. VDD must be powered up at the same time as VDDA.
2. VREFH must be powered up later than or at the same time as VDD/VDDA.

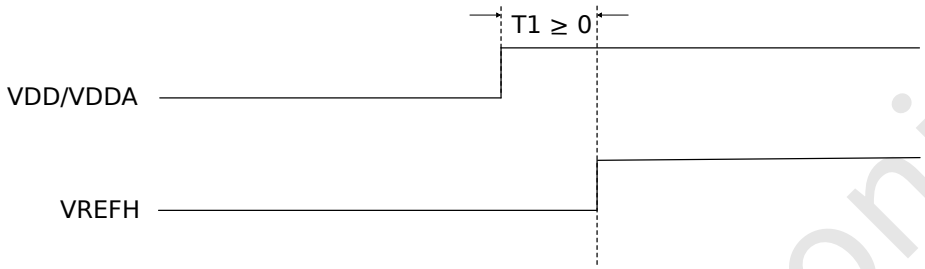
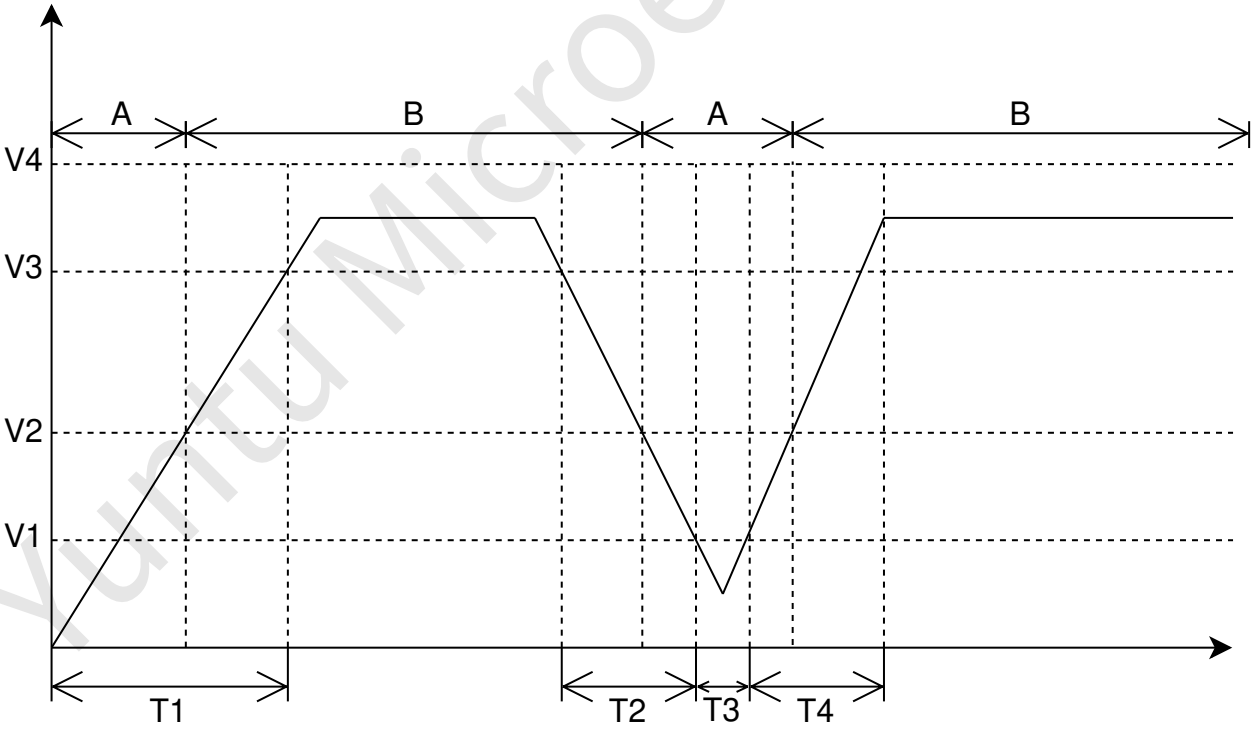


Figure 4: Power Up Sequence

6.2.9.2 Power Up Requirements

It is necessary to ensure that VDD/VDDA meets the following timing during the power-up process of YTM32B1LD0x.



A : There is no guarantee of proper functionality when the MCU is in uncertain status.

B : The MCU operates normally.

Figure 5: Power Up Requirements

Symbol	Name	Description	Unit (V)
V1	Restart threshold voltage	When restarting the MCU, VDD/VDDA should keep below V1 for a period of T3.	0.2
V2	Minimum MCU operating voltage	The MCU starts working when the power supply reaches V2.	1.8
V3	Lower voltage limit of MCU operating normally	Minimum operating voltage for normal MCU operation and interaction with peripherals.	2.7
V4	Upper voltage limit of MCU operating normally	Maximum operating voltage for normal MCU operation and interaction with peripherals	5.5

Symbol	Name	Description	Requirement
T1	Power up time	Rising time of MCU VDD/VDDA from 0V to V3	50 μs $<$ T1 $<$ 50ms
T2	Power down time	Drop time of MCU VDD/VDDA from V3 to V1 during the MCU restart/power down process	10 μs $<$ T2 $<$ 500ms
T3	Restart threshold voltage retain time	Minimum duration of MCU VDD/VDDA below V1, when restarting MCU	T3 $>$ 100 μs
T4	Restart power up time	Rising time of MCU VDD/VDDA normal operation from V1 to V3	50 μs $<$ T4 $<$ 50ms

NOTE: The power-up process needs to be restarted if a VDD/VDDA voltage drop occurs during the T1~T4 power-up process before the VDD/VDDA voltage reaches the V2 voltage. Restarting the power-up of MCU needs to ensure that the voltage of VDD/VDDA continues to drop below V1 and remains there for T3 time.

6.2.10 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance.

6.3 AC Characteristics

6.3.1 Device Clock Specifications

Symbol	Description	Min.	Max.	Unit	Notes
f_{core}	System and core clock	–	48	MHz	
f_{bus}	Bus clock	–	24	MHz	

6.3.2 I/O Electrical Characteristics

6.3.2.1 AC Electrical Characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and the rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

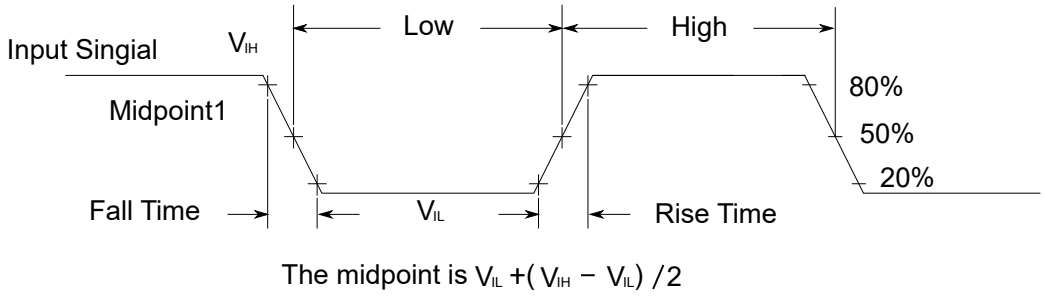


Figure 6: Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L = 30pF loads
- Normal drive strength

6.4 Peripheral Operating Requirements and Behaviors

6.4.1 EOSC(8-24MHz) Characteristics

The following diagram is External OSC circuit.

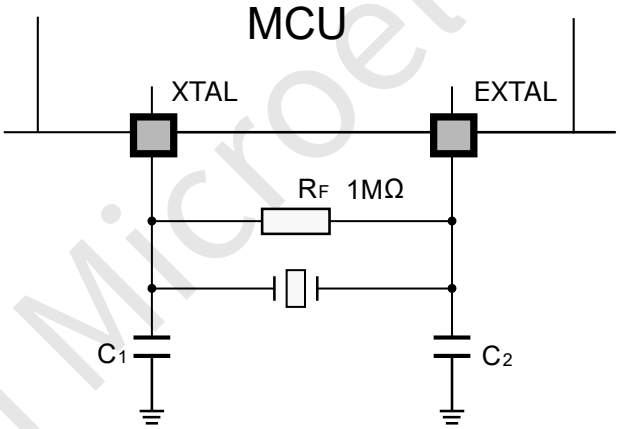


Figure 7: EOSC diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	–	5.5	V	
I_{DDOSC}	24MHz oscillator	–	2.3	–	mA	
V_{IH}	Input high voltage – EXTAL pin in external clock mode, V_{DD}=5V	3.8	–	V_{DD}	V	
	Input high voltage – EXTAL pin in external clock mode, V_{DD}=3.3V	2.2	–	V_{DD}	V	
V_{IL}	Input low voltage – EXTAL pin in external clock mode, V_{DD}=5V	V_{SS}	–	2.3	V	
	Input low voltage – EXTAL pin in external clock mode, V_{DD}=3.3V	V_{SS}	–	1.2	V	
T_{EOSCSU}	EOSC startup time (24MHz oscillator)	–	0.5	–	ms	

Table 17 continued from previous page

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
D_{EOSC}	Duty of EOSC (24MHz oscillator)	45	50	55	%	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	8MHz oscillator feedback resistor	–	–	–	MΩ	
	16MHz oscillator feedback resistor	–	–	–	MΩ	
	24MHz oscillator feedback resistor	–	–	–	MΩ	
V_{PP}	Peak-to-peak amplitude of oscillation (24MHz oscillator)	–	2.25	–	V	

1. Depending on the oscillator manual, $C_L = (C_1 * C_2/(C_1 + C_2)) + C_S$. For crystal load balance, $C_1 = C_2$. C_S is parasitic capacitors, C_L is load capacitor of oscillator, calculate C_1 and C_2 according to this formula.

6.4.2 FIRC(48MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{FIRC}	Fast internal reference frequency	–	48	–	MHz	
ACC_{FIRC}	FIRC frequency accuracy, factory trimmed, 25 °C	-1.0	–	1.0	%	
	FIRC frequency accuracy, factory trimmed, 0 °C – 85 °C	-1.5	–	1.5	%	
	FIRC frequence accuracy, factory trimmed, −40 °C – 105 °C	-2.5	–	2.5	%	
I_{FIRC}	FIRC operating current	–	770	–	μA	
$T_{Startup}$	Startup time	–	3	–	μs	

6.4.3 SIRC(128KHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SIRC}	Slow internal reference frequency	–	128	–	KHz	
ACC_{SIRC}	SIRC frequency accuracy, factory trimmed, 25 °C	-3.0	–	3.0	%	
	SIRC frequency accuracy, factory trimmed, 0 °C – 85 °C	-4.0	–	4.0	%	
	SIRC frequence accuracy, factory trimmed, −40 °C – 105 °C	-5.0	–	5.0	%	
I_{SIRC}	SIRC operating current	–	16	–	μA	
$T_{Startup}$	Startup time	–	10	–	μs	

6.4.4 ADC Characteristics

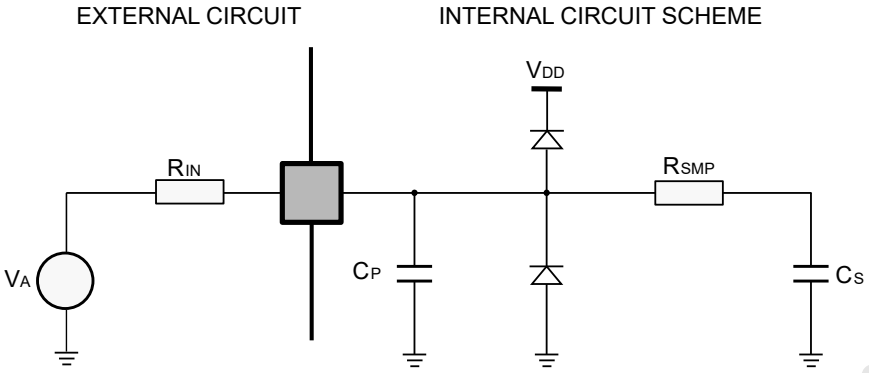


Figure 8: ADC circuit

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage		2.7	5.0	5.5	V	
I_{DDA}	Analog supply current		–	1.6	–	mA	
ΔV_{DDA}	V_{DD} - V_{DDA}		-100	–	100	mV	
V_{REFH}	Reference voltage		2.7	–	V_{DDA}	V	
I_{REFH}	Reference current		–	436	–	μA	
V_{IN}	Input voltage		0	–	V_{REFH}	V	
R_{SMP}	Sampling switch impedance		0.18	0.64	1.5	kΩ	
R_{IN}	Input impedance		–	200	–	kΩ	
C_P	Pin Capacitance		–	3	–	pF	
C_S	Sampling capacitance		–	6.5	–	pF	

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
$T_{STARTUP}$	Analog startup time		–	2	–	μs	
T_{SAMPLE}	Sampling time	ADC functional clock is 16MHz	4	–	–	cycles	
T_{CONV_12BIT}	Total conversion time with sample	ADC functional clock is 16MHz and select 12-bit resolution	–	16	–	cycles	
T_{CONV_10BIT}	Total conversion time with sample	ADC functional clock is 16MHz and select 10-bit resolution	–	14	–	cycles	
T_{CONV_8BIT}	Total conversion time with sample	ADC functional clock is 16MHz and select 8-bit resolution	–	12	–	cycles	

Table 21 continued from previous page

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
T_{CONV_6BIT}	Total conversion time with sample	ADC functional clock is 16MHz and select 6-bit resolution	–	10	–	cycles	

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
DNL	Differential nonlinear	12-bit resolution	–	±1.0	–	LSB	
INL	Integer nonlinear	12-bit resolution	–	±2.5	–	LSB	
E_{GAIN}	Gain error	12-bit resolution	–	1.5	–	LSB	
E_{OFFSET}	Offset error	12-bit resolution	–	3.5	–	LSB	
ENOB	Effective number bits	12-bit resolution	–	10.5	11.0	Bits	
SINAD	Signal-to-noise-and-distortion ratio	12-bit resolution	–	65.0	68.0	dB	

6.4.5 ACMP Characteristics

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage		2.7	5.0	5.5	V	
I_{DDA}	Analog supply current		–	30	–	μA	
$V_{INOFFSET}$	Analog input offset voltage		-10	–	10	mV	
V_{IN}	Analog input voltage		0	–	V_{DDA}	V	
V_{HYST0}	Analog comparator hysteresis 0		–	20	–	mV	
V_{HYST1}	Analog comparator hysteresis 1		–	40	–	mV	

6.4.6 NVM Specifications

6.4.6.1 Flash Command Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T_{pgm}	Program execution time	46	50	53.5	μs	
T_{erase}	Erase execution time	4.0	4.5	5.0	ms	
T_{chip_erase}	Chip erase execution time	30	35	40	ms	

6.4.6.2 Flash High Voltage Current Behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_PGM}	Average current adder during high voltage flash programming operation	–	2.3	4	mA	
I_{DD_ERS}	Average current adder during high voltage flash erase operation	–	1.23	2	mA	

6.4.6.3 Reliability Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{nvmretp}$	Data retention	100	–	–	years	
$t_{nvmcycp}$	Cycling endurance	100,000	–	–	cycles	

6.4.7 Debug Module Electrical

6.4.7.1 SWD Electrical Specifications

Table 27: SWD full voltage range electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

6.4.7.2 SWD Input Clock Timing

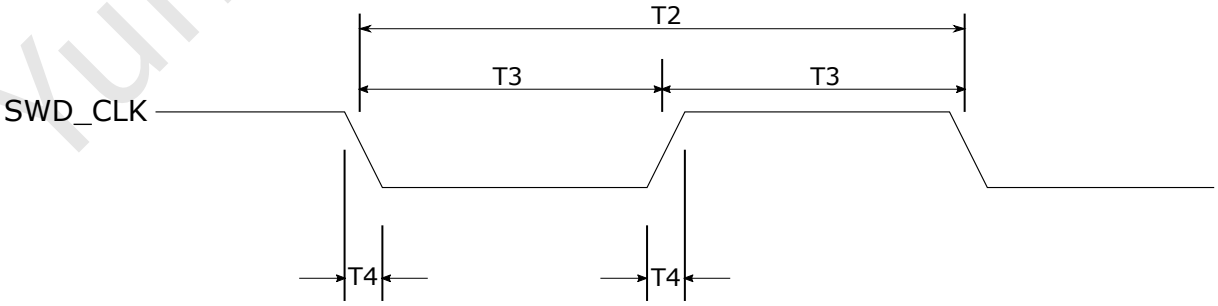


Figure 9: SWD Clock Timing

6.4.7.3 SWD Output Data Timing

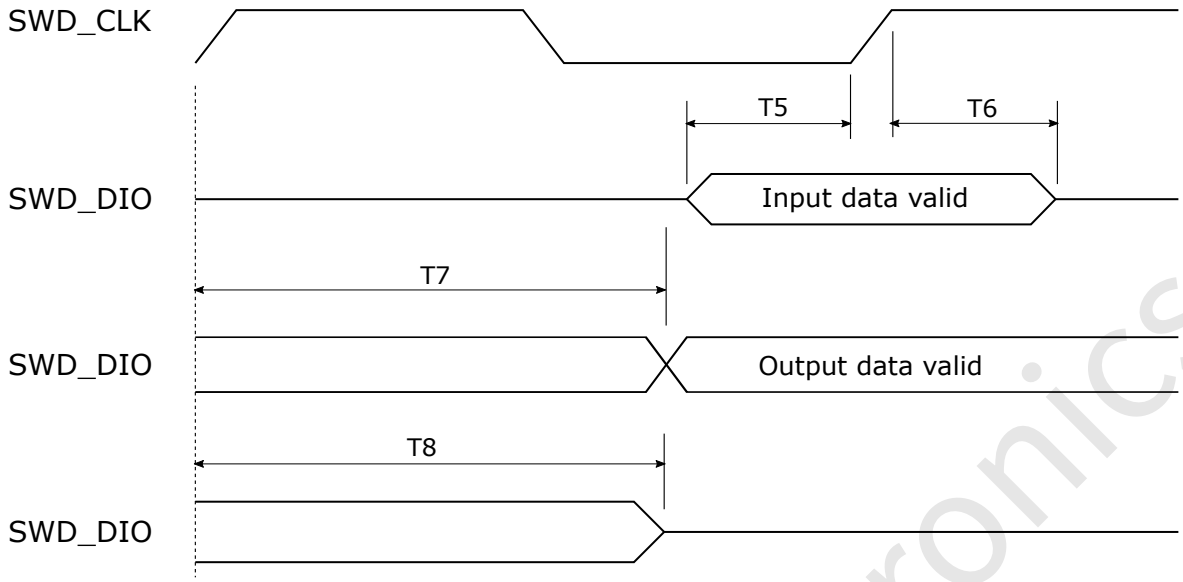


Figure 10: SWD Data Timing

6.5 Thermal Attributes

Table 28: Thermal Characteristics

Package Family	Package Type	Thermal Resistance JA (°C/W)
	LQFP32L	89
	LQFP48L	78
	LQFP64L	76

7 Pinouts$_{LQFP}$

7.1 IO Signal Description

The pinouts signal description is as follows:

Table 29: Pinmux Table

64 LQFP	48 LQFP	32 LQFP	NAME	ALT0[1]	ALT1[2]	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	1	PTD1	-	PTD1	eTMR0_CH3	SPI1_SDI	-	I2C1_SCL	-	-
2	2	2	PTD0	-	PTD0	eTMR0_CH2	SPI1_SCK	-	I2C1_SDA	-	-
3	-	-	PTE11	-	PTE11	-	lpTMR0_ALT1	-	-	-	-
4	-	-	PTE10	-	PTE10	-	RTC_CLKOUT	-	-	-	-[3]
5	3	-	PTE5	-	PTE5	TCLK_IN2	-	-	CAN0_TX	-	-
6	4	-	PTE4	-	PTE4	-	-	-	CAN0_RX	-	-
7	5	3	VDD	-	-	-	-	-	-	-	-

64 LQFP	48 LQFP	32 LQFP	NAME	ALT0[1]	ALT1[2]	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
8	6	4	VDDA	-	-	-	-	-	-	-	-
9	-	-	VREFH	-	-	-	-	-	-	-	-
-	-	5	VREFL	-	-	-	-	-	-	-	-
10	7	6	VSS	-	-	-	-	-	-	-	-
11	8	7	PTB7	EXTAL	PTB7	I2C0_SCL	-	-	-	-	-
12	9	8	PTB6	XTAL	PTB6	I2C0_SDA	-	-	-	-	-
13	-	-	PTE3	-	PTE3	eTMR0_FLT0	-	-	-	-	ACMP0_OUT
14	10	-	PTD16	-	PTD16	eTMR0_CH1	-	SPI0_SDI	-	-	-
15	11	-	PTD15	-	PTD15	eTMR0_CH0	-	SPI0_SCK	-	-	-
16	12	-	PTE9	-	PTE9	eTMR0_CH7	-	-	-	-	-
17	13	-	PTE8	ACMP0_IN3	PTE8	eTMR0_CH6	-	-	-	-	-
18	14	9	PTB5	-	PTB5	eTMR0_CH5	SPI0_PCS1	SPI0_PCS0	CLKOUT	-	-
19	15	10	PTB4	ADC0_SE15	PTB4	eTMR0_CH4	SPI0_SDO	-	-	-	-
20	16	11	PTC3	ADC0_SE13 ACMP0_IN4	PTC3	eTMR0_CH3	CAN0_TX	UART0_TX	-	-	-
21	17	12	PTC2	ADC0_SE5 ACMP0_IN5	PTC2	eTMR0_CH2	CAN0_RX	UART0_RX	-	-	-
22	-	-	PTD7	ACMP0_IN6	PTD7	UART2_TX	-	-	-	-	-
23	-	-	PTD6	ACMP0_IN7	PTD6	UART2_RX	-	-	-	-	-
24	18	-	PTD5	-	PTD5	-	lpTMR0_ALT2	SPI2_PCS2	-	-	-
25	19	13	PTC1	ADC0_SE12	PTC1	eTMR0_CH1	-	SPI2_PCS1	-	-	-
26	-	14	PTC0	ADC0_SE4	PTC0	eTMR0_CH0	-	SPI2_PCS0	-	-	-
27	-	-	PTC17	-	PTC17	-	-	SPI2_SDO	-	-	-
28	20	-	PTC16	ADC0_SE7	PTC16	-	-	SPI2_SDI	-	-	-
29	21	-	PTC15	ADC0_SE14	PTC15	eTMR2_CH1	-	SPI2_SCK	-	-	-
30	22	-	PTC14	ADC0_SE6	PTC14	eTMR2_CH0	-	-	-	-	-
31	23	15	PTB3	ADC0_SE11	PTB3	eTMR1_CH1	SPI0_SDI	-	-	-	-
32	24	16	PTB2	ADC0_SE3	PTB2	eTMR1_CH0	SPI0_SCK	-	-	-	-
33	25	17	PTB1	ADC0_SE10	PTB1	UART0_TX	SPI0_SDO	TCLK_IN0	CAN0_TX	-	-
34	26	18	PTB0	ADC0_SE2	PTB0	UART0_RX	SPI0_PCS0	lpTMR0_ALT3	CAN0_RX	-	-
35	27	-	PTC9	-	PTC9	UART1_TX	-	-	-	-	-
36	28	-	PTC8	-	PTC8	UART1_RX	-	-	-	-	-
37	29	19	PTA7	ADC0_SE9	PTA7	eTMR0_FLT2	-	-	-	-	-
38	-	20	PTA6	ADC0_SE1	PTA6	eTMR0_FLT1	SPI1_PCS1	-	-	-	-
39	-	-	PTE7	-	PTE7	eTMR0_CH7	SPI1_PCS2	-	-	-	-
40	30	-	VSS	-	-	-	-	-	-	-	-
41	31	-	VDD	-	-	-	-	-	-	-	-
42	32	-	PTB13	-	PTB13	eTMR0_CH1	-	-	-	-	-
43	-	-	PTB12	-	PTB12	eTMR0_CH0	-	-	-	-	-
44	-	-	PTD4	-	PTD4	eTMR0_FLT3	-	-	-	-	-
45	33	21	PTD3	-	PTD3	-	SPI1_PCS0	-	-	-	NMI_b
46	34	22	PTD2	-	PTD2	-	SPI1_SDO	-	-	-	-
47	35	23	PTA3	-	PTA3	-	I2C0_SCL	-	-	UART0_TX	-
48	36	24	PTA2	-	PTA2	-	I2C0_SDA	-	-	UART0_RX	-

64 LQFP	48 LQFP	32 LQFP	NAME	ALT0[1]	ALT1[2]	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
49	37	25	PTA1	ADC0_SE8 ACMP0_IN1	PTA1	eTMR1_CH1	-	-	-	-	-
50	38	26	PTA0	ADC0_SE0 ACMP0_IN0	PTA0	-	-	-	-	-	-
51	39	27	PTC7	-	PTC7	UART1_TX	-	-	CAN0_TX	-	-
52	40	28	PTC6	-	PTC6	UART1_RX	-	-	CAN0_RX	-	-
53	-	-	PTE6	-	PTE6	SPI0_PCS2	-	-	-	-	-
54	-	-	PTE2	-	PTE2	SPI0_SDO	lpTMR0_ALT0	-	-	-	-
55	41	-	PTA13	-	PTA13	-	-	I2C1_SCL	UART2_TX	-	-
56	42	-	PTA12	-	PTA12	-	-	I2C1_SDA	UART2_RX	-	-
57	43	-	PTA11	-	PTA11	-	-	-	-	-	-
58	44	-	PTA10	-	PTA10	-	-	-	-	-	-
59	-	-	PTE1	-	PTE1	SPI0_SDI	-	-	SPI1_PCS0	-	-
60	-	-	PTE0	-	PTE0	SPI0_SCK	TCLK_IN1	-	SPI1_SDO	-	-
61	45	29	VDD15	-	-	-	-	-	-	-	-
62	46	30	PTC4	ACMP0_IN2	PTC4	eTMR1_CH0	-	-	-	-	SWD_CLK
63	47	31	PTA5	-	PTA5	-	TCLK_IN1	-	-	-	RESET_b
64	48	32	PTA4	-	PTA4	-	-	ACMP0_OUT	-	-	SWD_IO

1. ALT0 is default mux mode of pin
2. ALT1 is GPIO mux mode
3. This pin can not be used during boot up

7.2 Packages

The information of package pinouts is as follows:

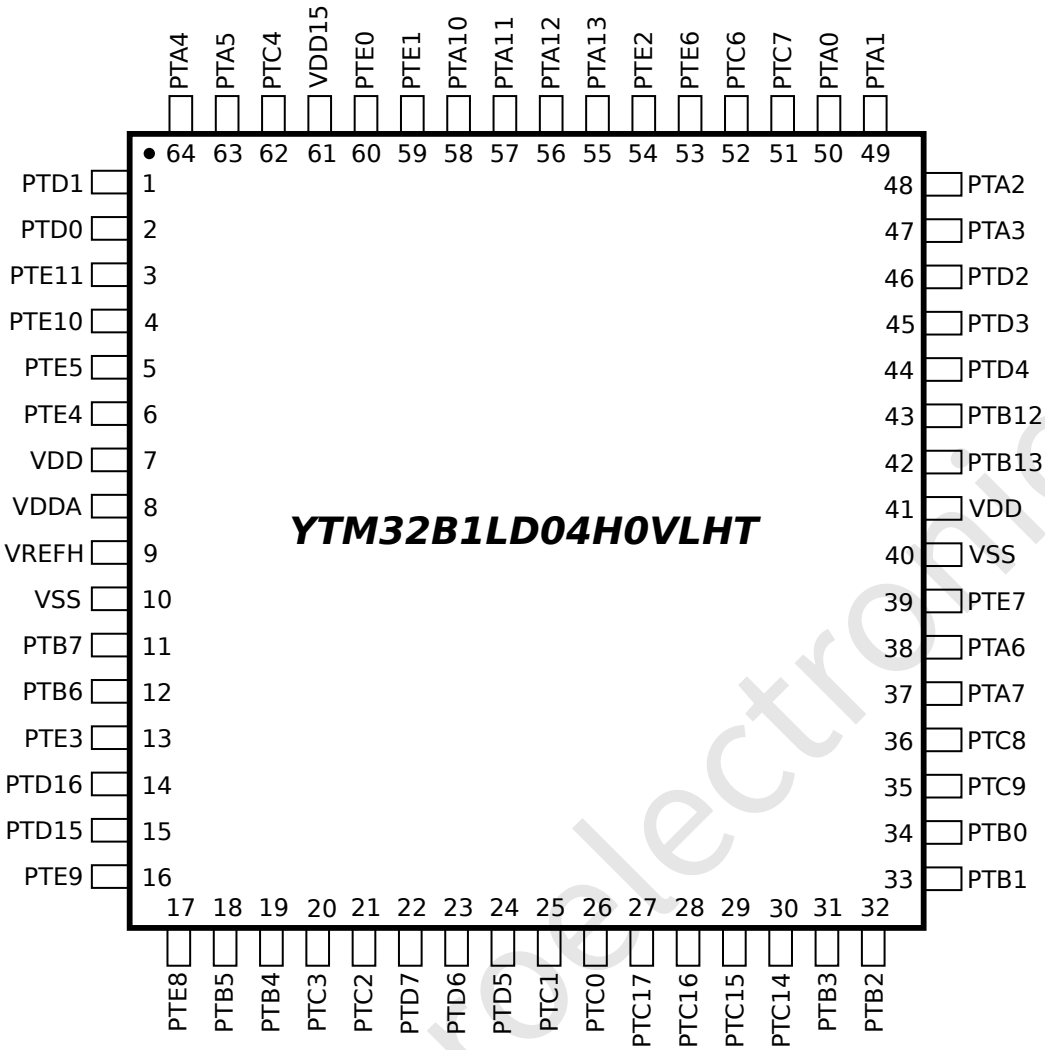


Figure 11: 64-pin LQFP package

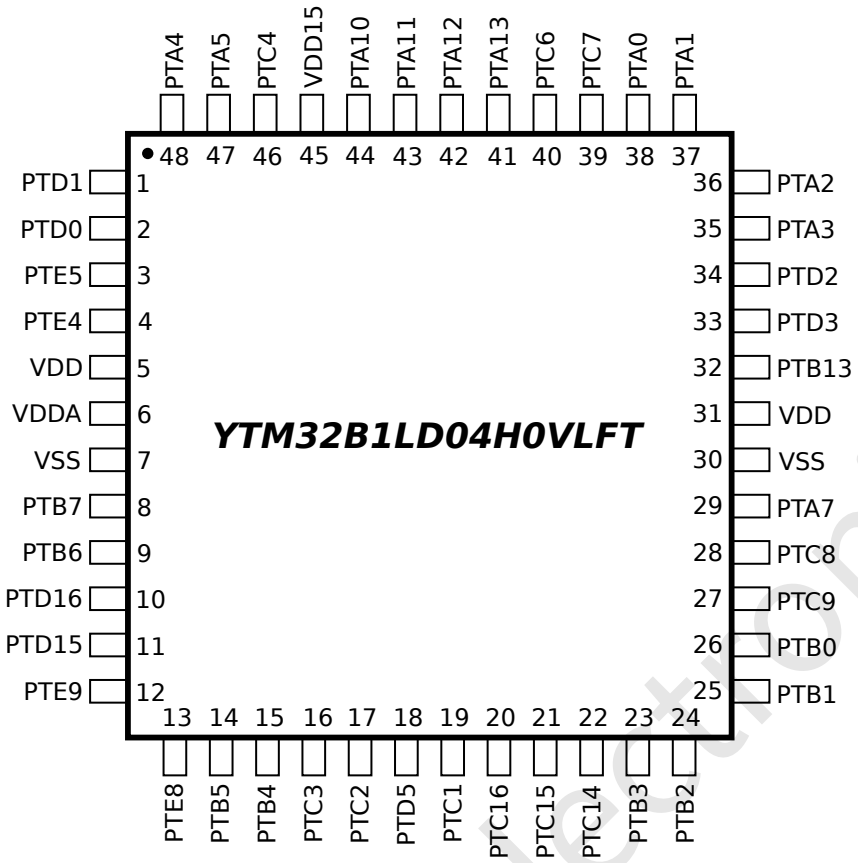


Figure 12: 48-pin LQFP package

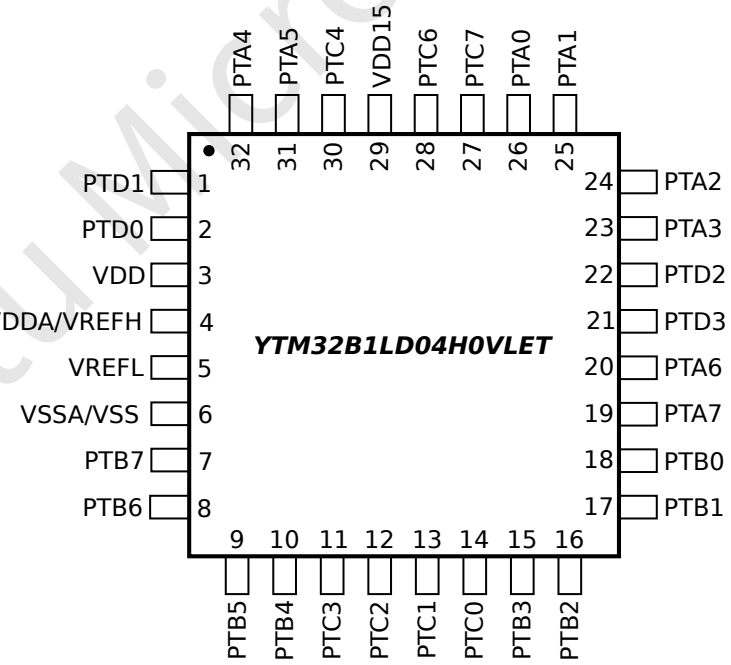
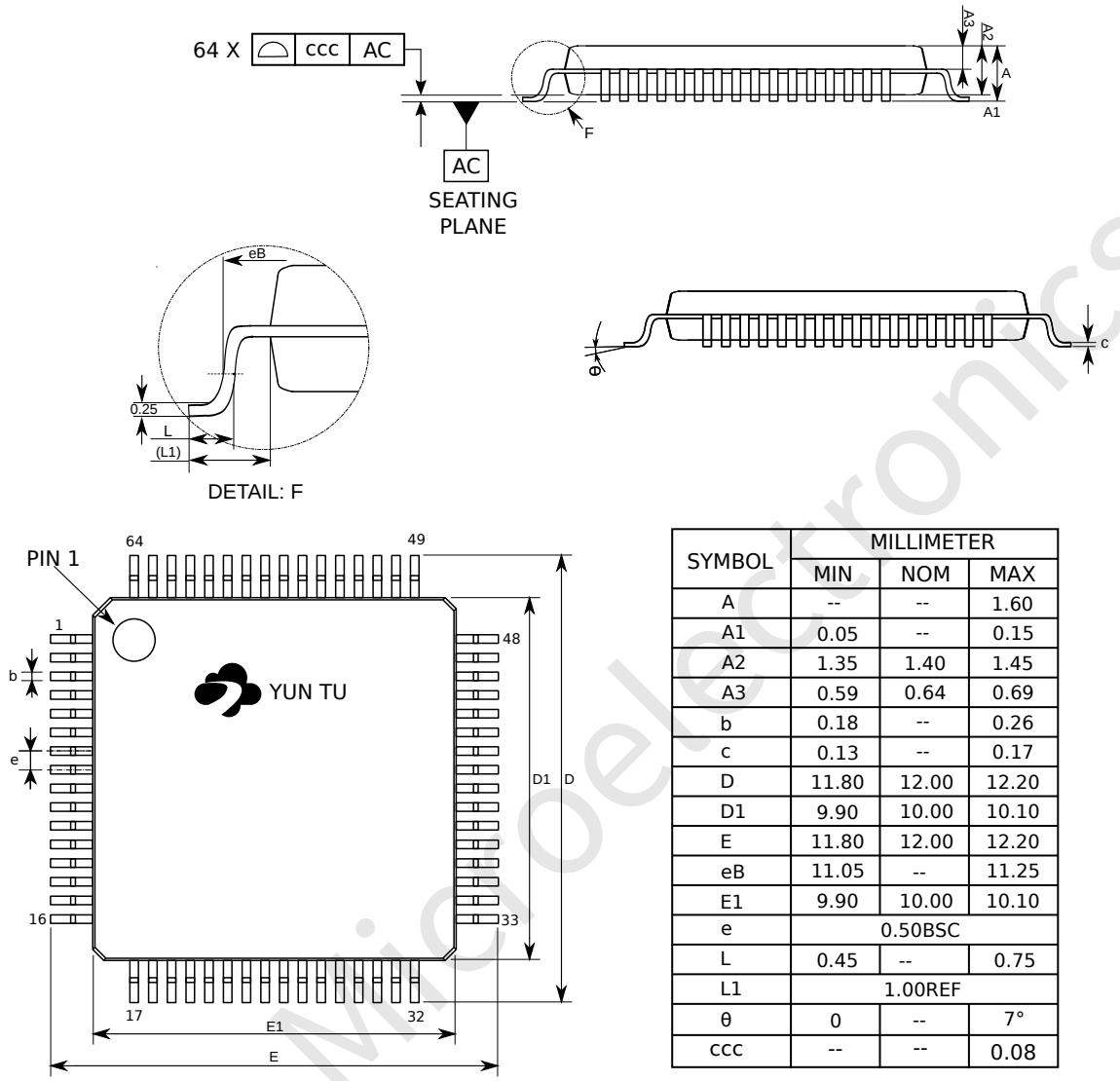


Figure 13: 32-pin LQFP package

Note: The chip mark will not contain packing information(T/R)

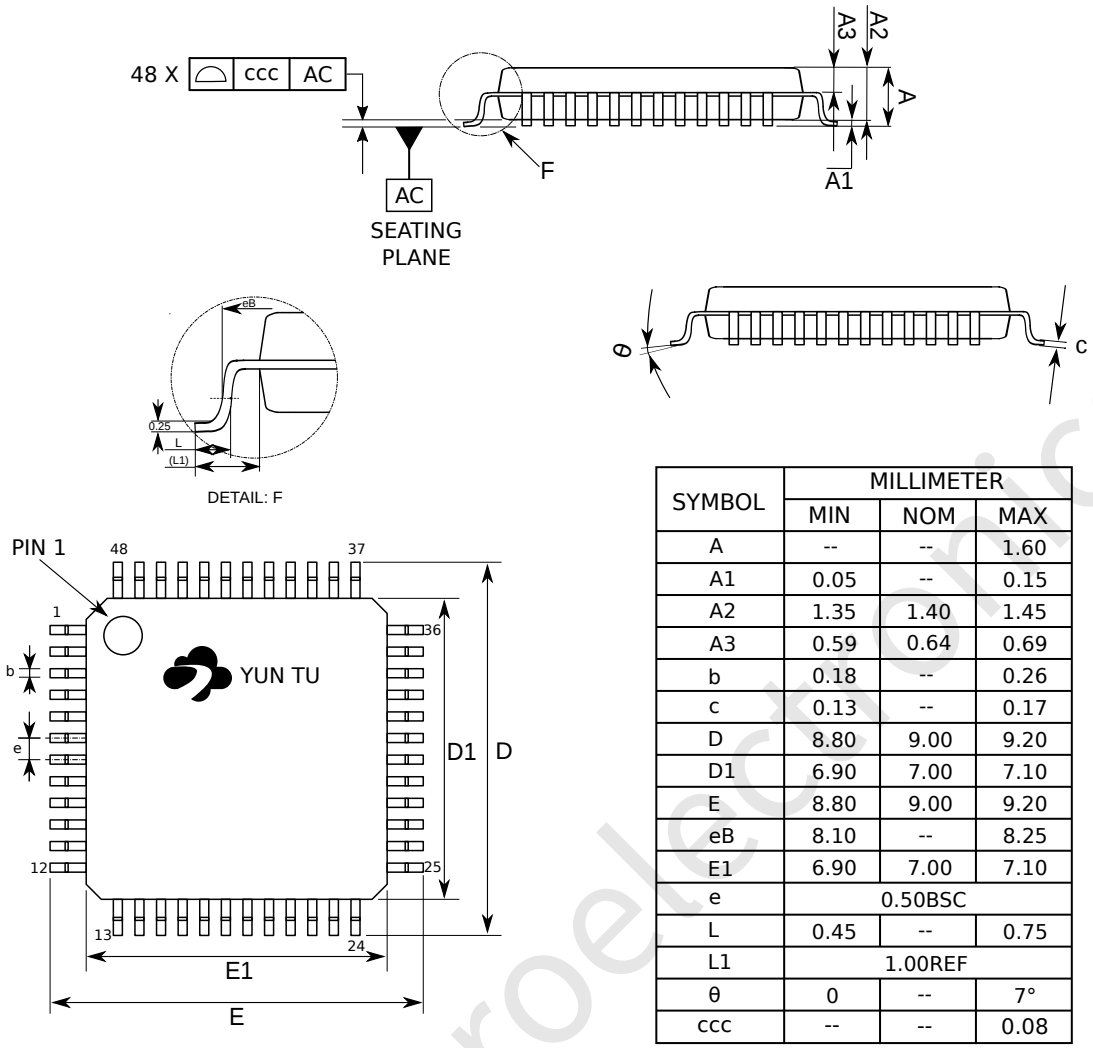
7.3 Dimensions

Package dimensions are as follows:



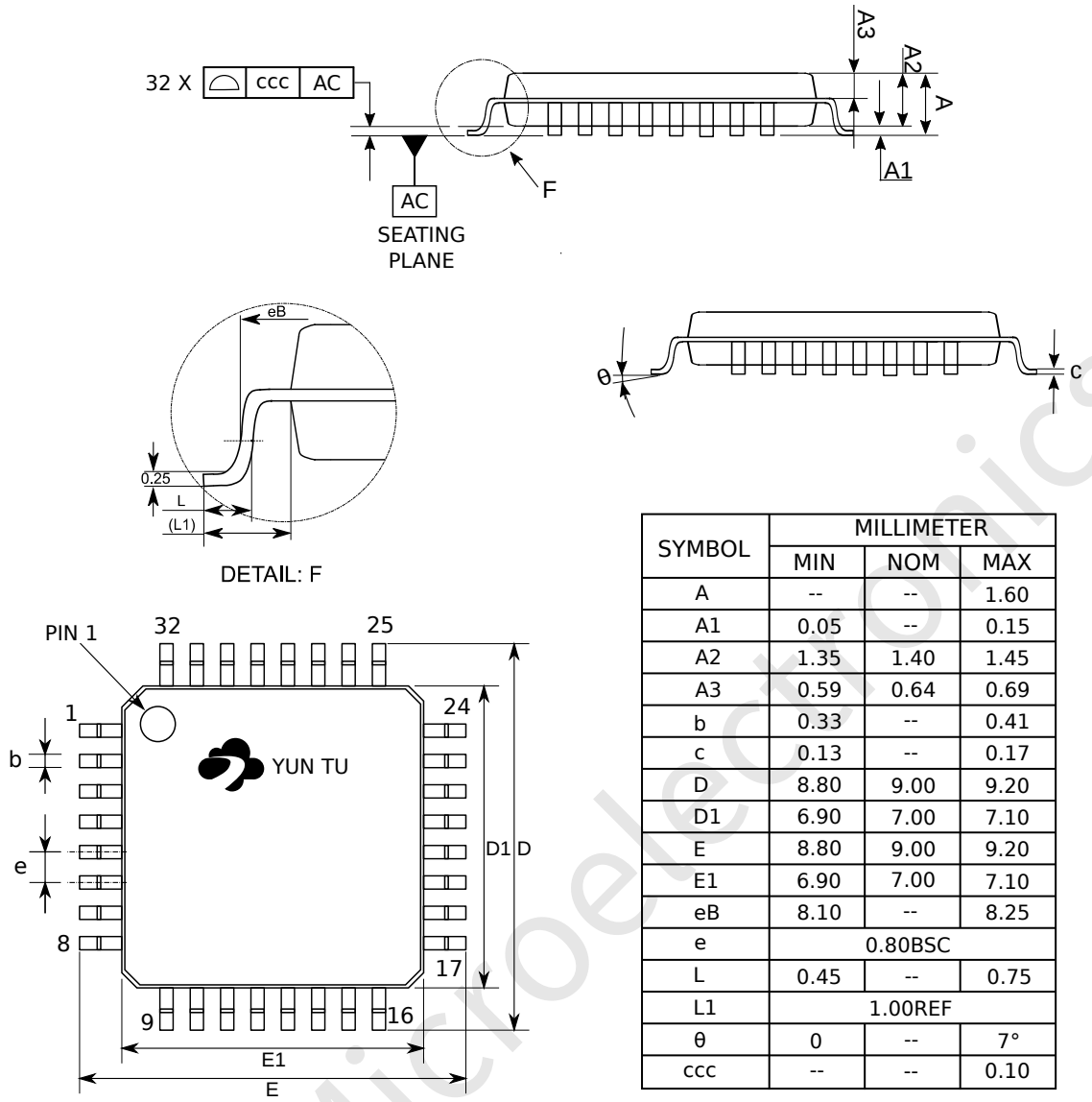
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
c	0.13	--	0.17
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.05	--	11.25
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°
ccc	--	--	0.08

Figure 14: 64pin LQFP



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
c	0.13	--	0.17
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
eB	8.10	--	8.25
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°
ccc	--	--	0.08

Figure 15: 48pin LQFP



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	--	0.41
c	0.13	--	0.17
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	--	8.25
e	0.80BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°
ccc	--	--	0.10

Figure 16: 32pin LQFP

Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2021/09/24	Initial version
1.1	2021/11/23	Modified 10K cycles as 100,000 cycles in flash cycles endurance
1.2	2021/12/17	Added power signal in Pinout decoupling
1.3	2022/01/23	Added AEC-Q100 information
1.4	2022/02/10	Fixed ADC channel numbers in Ordering parts chapter
1.5	2022/08/15	Fixed ADC channel numbers in Features Updated Flash data retention description
1.6	2023/03/15	Added the new chapter of Features Updated $T_{J\ C}$ to $T_{J\ V}$ and $T_{J\ V}$ to $T_{J\ M}$ in the section of Thermal Operating Characteristics Updated the contents in the section of ESD Handling Ratings Updated I_{OH} to I_{OL} of V_{OL} in the section of DC Electrical Specifications at 3.3V Updated I_{OH} to I_{OL} of V_{OL} in the section of DC Electrical Specifications at 5.0V Updated the description of FIRC and EOSC in the section of Power Consumption Added the new section of Power Sequence Updated the contents in the section of Reliability Specifications Added the new section of Thermal Attributes Updated the Pinmux Table in the section of IO Signal Description
1.7	2023/7/21	Added the new section of Power Up Requirements Added the coplanarity specifications of product in the section of Dimensions Added the location information of PIN 1 in the section of Dimensions

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