YTM32B1MD1x Data Sheet

Support: YTM32B1MD14G0MLLT, YTM32B1MD14G0MLHT, YTM32B1MD14G0MLHIT

Document Number: YTM32B1MD1x DS

Rev.1.5, 2023/6/28

1 Features Summary

- AEC-Q100 qualified
- ASIL B compliant
- 32-bit Cortex-M33 with FPU and DSP, up to 120 MHz
- Up to 256 KB * 2 Program Flash
  - Support ECC feature
  - Support OTA
- Up to 64 KB SRAM
  - Support ECC feature
  - Two 16 KB SRAM blocks support data retention in Powerdown mode
- 32 bytes register file which supports data retention in Powerdown mode
- Provide multiple clock sources including:
  - 96 MHz Fast Internal RC Oscillator (FIRC)
  - 12 MHz Slow Internal RC Oscillator (SIRC)
  - 4~40 MHz Fast Crystal Oscillator (FXOSC)
  - Up to 120 MHz Phase-Locked Loop (PLL)
- Power Control Unit (PCU) with internal regulators capable of supporting multiple power modes including:
  - Active
  - Sleep
  - Deepsleep
  - Standby
  - Powerdown
- Support up to 16 WKU pins, RESET_b pin and 4 module interrupts to wake up from Powerdown mode
- 16 DMA channels with up to 52 hardware trigger sources
- Human-machine interface
  - Up to 87 general-purpose input/output (GPIO)
  - External interrupt
- Analog modules providing precision mixed-signal capabilities, including:
  - One 12-bit, 2Msps SAR ADC, up to 32 external channels and 6 internal channels
  - On-chip Analog Comparator (ACMP) with 8-bit DAC, up to 8 channels
  - Support temperature sensor
- Timers
  - One Timer (TMR)
  - One 4-channel Periodic Timer (pTMR)
  - One Low Power Timer (lpTMR)
  - Four 8-channel Enhanced Timer (eTMR)
  - One Real Time Clock (RTC)
  - One Programmable Trigger Unit (PTU)
- Serial communication interfaces
  - Three FlexCAN modules with FD
  - Three LINFlexD modules
  - Four SPI modules
  - Two I2C modules
  - One SENT module
- I/O supporting 2.97 ~ 5.5 V supply
- Wide operating voltage ranges (2.97 ~ 5.5 V) with fully functional flash memory program/erase/read operations
- Temperature range:
  - Ambient operating temperature: -40 °C ~ 125 °C
  - Junction operating temperature: -40 °C ~ 150 °C
- Security and Safety features are supported as follows:
  - Cyclic Redundancy Checker (CRC)
  - Hardware Cryptography Unit (HCU) which supports AES-128
  - True Random Number Generator (TRNG)
  - Clock Monitor Unit (CMU)
  - Watchdog (WDG)
  - External watchdog (EWDG)
  - MPU for dynamic task protection (16 regions)
  - ECC Management Unit (EMU)
- Debug functionality
  - Joint Test Action Group (IEEE 1149.1 standard)
  - Serial Wire Debug (SWD)
- Package options
  - 100-pin LQFP
  - 64-pin LQFP

Contents

2 Overview

YTM32B1MD1x series provide the highly scalable portfolio of ARM® Cortex®-M33 MCUs in the automotive industry with the Arm Cortex-M33 core at higher frequency, more memory, ASIL-B rating and advanced security module. With 2.97 ~ 5.5 V supply and focus on exceptional EMC/ESD robustness, YTM32B1MD1x series devices are well suited to a wide range of applications in electrical harsh environments, and are optimized for cost-sensitive applications offering low pin-count option.

The YTM32B1MD1x series offer a broad range of memory, peripherals and package options. They share common peripherals and pin counts allowing developers to migrate easily within an MCU family or among the MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the YTM32B1MD1x series for their end product platforms, maximizing hardware and software reuse and reducing time-to-market.

3 Block Diagram

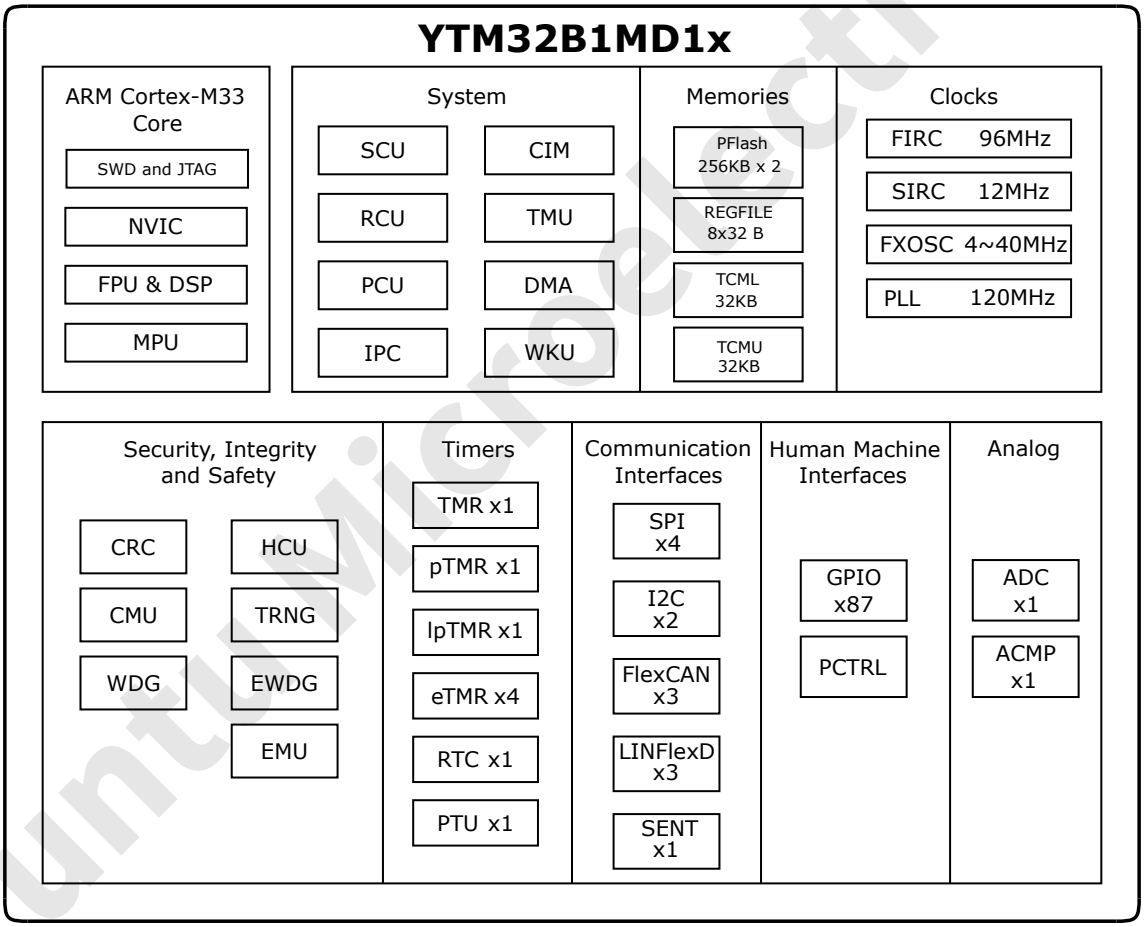


Figure 1: YTM32B1MD1x Block Diagram

4 Features

The following sections describe the high-level module features for YTM32B1MD1x device.

4.1 Core Modules

4.1.1 ARM Cortex-M33

- ARM Cortex M33 core running up to 120 MHz
- ARMv8-M MPU for dynamic task protection (16 regions)
- Single cycle 32 x 32 bits multiply
- 3-stage pipeline, thumb-2 technology
- Digital Signal Processor (DSP)
- Single Precision Floating Point Unit (FPv5), IEEE 754 compliant
- Support for the instruction trace option:
  - Embedded Trace Macrocell (ETM)
- Binary compatible instruction set with the ARM Cortex M4/M7

4.1.2 Nested Vector Interrupt Controller (NVIC)

- 8 priority levels
- Up to 110 interrupt sources
- Includes a single non-maskable interrupt

4.1.3 Debug Controller

- 2-pin serial wire debug (SWD) provides external debugger interface
- Support JTAG port (IEEE 1149.1 standard)
- Support ITM(Instruction Trace Macrocell): S/W Instrumentation Messaging + Simple Data Trace Messaging + watch points Messaging
- Support ETM(Embedded Trace Macrocell): Used for instruction trace
- Support DWT(Data and Address Watch points): 8 flash breakpoints and 4 data watch points

4.2 System Modules

4.2.1 System Clock Unit (SCU)

- SCU provides system clock divider to generate core clock, fast bus clock and slow bus clock
- SCU provides glitch free switcher to select system clock source
- Fast internal RC oscillator(FIRC)
  - Up to 96MHz
  - Default system boot clock source
  - Support trim for temperature and process
  - Can be selected as PLL reference clock
- Slow internal RC oscillator(SIRC)
  - Can be selected as system clock source
  - Always on unless it is forced to be disabled in Standby mode and Powerdown mode
  - Support trim for temperature and process
- Fast crystal oscillator(FXOSC)
  - Support 4~40MHz crystal
  - Can be selected as PLL reference clock
  - Can be selected as system clock source
- Phase-locked loop(PLL)
  - Up to 120 MHz

- Contain voltage-controlled oscillator(VCO)
- Support selectable reference clock
- Contain Frequency lock detector
- Can be selected as system clock source

4.2.1.1 Clock Monitor Unit (CMU)

- SCU contains 4 CMU blocks
- CMU monitors slow bus clock, FIRC, FXOSC and PLL clock
- FXOSC or SIRC clock can be selected as reference clock of CMU
- CMU can detect frequency out of range, loss of checked clock and loss of reference clock

4.2.2 Power Control Unit (PCU)

- Combination of internal and external voltage regulator options, offering a variety of power modes
- Active POR providing brown-out detect
- Low voltage reset for all system relevant power domains (LVR)
- High voltage detect (HVD) as indication for software

4.2.3 Reset Controller Unit (RCU)

- Record the reset sources of most recent resets
- Configurable filter for reset pin
- Reset pin filter can work in all power modes

4.2.4 IP Controller (IPC)

- Support software reset to peripheral
- Peripheral Bus clock enable
- IPC clock source selection as follows
  - PLL 120MHz
  - FIRC 96 MHz
  - SIRC 12 MHz
  - FXOSC 4~40 MHz
- IPC clock divide values from 1 to 16

4.2.5 Wakeup Unit (WKU)

- Support up to 16 external input pins and RESET_b pin to wake up from Powerdown mode
- Support up to 4 internal interrupts with individual enable bits for MCU to wake up from Powerdown mode
- Input sources may be external pins or from internal modules capable of running in Powerdown mode
- External input pins are programmable for falling-edge, rising-edge, or any-edge detection
- Support to enable external input pin and filter detection in Powerdown mode
- Optional digital filters are provided to qualify an external pin detect. When the SIRC clock is disabled, filters are disabled and bypassed

4.2.6 Direct Memory Access (DMA)

- All address range data transfer from source to destination

- Support separate source/destination data size configuration
  - Word(32-bit), half word(16-bit), byte(8-bit) transfer size
- Support separate source/destination address offset configuration
  - Address increase/decrease/not change selectable
- Up to 16 DMA channels
  - Fix priority and round-robin arbitration
  - Support channel to channel link
- Software/Hardware trigger
- Up to 52 peripheral hardware triggers
- Internal data FIFO for data transfer
- Support update DMA transfer information from system memory after transfer complete
- Support data transfer loop and trigger loop

4.2.7 Trigger Multiplex Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources
- Support up to 12 trigger input pads and up to 8 trigger output pads

4.2.8 Chip Integration Module (CIM)

- System function configuration
- ADC/ACMP trigger synchronize selection
- Software trigger generation
- eTMR external clock and fault selection
- FPU interrupt enable
- System unique device identification (UID)
- Flash memory and system RAM size configuration
- Package configuration
- FlexCAN FD feature configuration

4.3 Memories

4.3.1 Embedded Flash Module (EFM)

- 512 KB PFlash with 8-bit ECC includes 2 blocks, block size is 256 KB, sector size is 1KB
- There are 2 NVR sectors with 8-bit ECC that includes secured AES key storage, One-Time-Program and Security control, each sector is 1KB
- Protection scheme against accidental program or erase operations
- Optional interrupt on command completion and status update
- Program and erase operations do not require any special power sources other than the normal VDD supply
- Support chip erase by debugger

4.3.2 Register File (REGFILE)

- 32 bytes regfile which supports data retention in Powerdown mode

4.3.3 On-chip SRAM

- 32 KB TCML and 32 KB TCMU

- Support ECC feature
- Two regions of 16KB SRAM which supports data retention in Powerdown mode

4.4 Analog

4.4.1 Analog-to-Digital Converter (ADC)

- Support up to 32 analog external input channels, and 6 internal channels
- Support 12-bit, 10-bit, 8-bit, and 6-bit single-ended configurable resolution
- Up to 2Msps for 12-bit resolution conversion performance
- Support DMA and conversion result FIFO with watermark
- Support multiple conversion modes
  - Single mode
  - Continuous mode
  - Discontinuous mode
- Support software/hardware trigger for ADC start conversion
- Support two low power modes
  - Wait mode: prevent ADC overrun when FIFO is full
  - Auto off mode: automatic control ADC power off
- Support watchdog for conversion result monitoring
- Support interrupt generate
  - Ready for conversion
  - End of sampling
  - End of conversion
  - End of sequence conversion
  - Overrun event
  - Watchdog event
- Support work and wake up when the chip under low power mode

4.4.2 Analog Comparator (ACMP)

- Up to 8 channels
- Operational over the entire supply range
- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable inversion on comparator output
- Function mode:
  - Common mode
  - Sample mode
  - Window mode
  - Continuous mode
    - One-shot mode
    - Loop mode
- All channels can be used to execute automatic comparison
- Support digital filter, the filter can be bypassed
- Two software selectable performance levels
  - Shorter propagation delay at the expense of higher power
  - Low power with longer propagation delay
- Functional in all power mode
- Support independent 8-bit DAC output to the comparator

- Support several interrupts
  - For common/sample/window mode
    - Generate interrupt on rising-edge, falling-edge or both edges of the comparator output
  - For continuous mode
    - Generate interrupt when the comparison results don't match with expectations
- Interrupt can generate without any clock except in continuous mode
- A comparison event can be selected to trigger DMA transfer

4.5 Timers

4.5.1 Timer (TMR)

- One 32-bit count-up timer with an 8-bit prescaler
- Four 32-bit compare channels
- An independent interrupt source for each channel
- Ability to stop the timer in debug mode

4.5.2 Periodic Timer (pTMR)

- Timers can generate interrupts
- Four channels of 32-bit timers, each timer has its independent timeout period and interrupt
- Ability to stop in debug mode
- Support chain mode to connect multiple timer to a longer timer

4.5.3 Low Power Timer (lpTMR)

- 16-bit time counter or pulse counter with compare
- Optional interrupt can generate asynchronous wakeup from any low power mode
- Hardware trigger output
- Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

4.5.4 Enhanced Timer (eTMR)

This chip contains 4 eTMRs (eTMR0~3), features of them can be divided into common features and individual features.

The common features of all eTMRs are listed below:

- Each eTMR has an independent 16-bit counter with a clock prescaler
- Configurable initial and final counter values
- Contain 8 channels
- Support two clock sources
  - Bus clock
  - External clock
- Support 7-bits clock prescaler
- Support three channel modes
  - PWM mode
    - Independent mode for each channel

        * Convenient generation of center aligned PWM
        * Complementary mode for each pair of channels
            · All channels support independent deadtime insertion
        * Support dithering
        * Channel output control (initialization, software control, mask control, double switch control, fault control)
            · Support 4 fault input sources
            · Support fault input from TMU or pad
            · Support fault input polarity control
            · Support fault input filter
            · Support fault input stretch
            · Support fault event generated by combinational logic
        * Relevant registers have buffer registers and support loading mechanism
    - Output Compare mode
        * The output can be configured to set, clear or toggle on match point
    - Input Capture mode
        * Support rising edges, falling edges or dual edges capture
        * Support input filter with a prescaler
        * Support capture test mode
        * Support pulse width measure
- Support generating triggers
    - Output triggers with adjustable pulse width on match point
    - Output pulse with adjustable width by PWM
- Polarity control is available for each channel
- Support GTB (Global Time Base)
- Support several interrupts
    - Channel interrupt (capture interrupt and compare interrupt)
    - Counter overflow interrupt
    - Fault event interrupt
- Support DMA
- Support counter running under debug mode

The individual features are listed below:

- eTMR1 and eTMR2 support quadrature decoder mode
    - Contain an independent 16-bit counter with a clock prescaler
    - Support 4 up-down counting modes
    - Support phase A and phase B input filter
    - Support quadrature decoder counter overflow interrupt
- eTMR0 and eTMR3 support modulated output
- eTMR2 supports hall sensor input
- eTMR1 and eTMR2 support input from ACMP

4.5.5 Real Time Clock (RTC)

- 32-bit seconds counter with overflow flag and optional interrupt
- Configurable 32-bit alarm
- 16-bit prescaler with compensation that can correct errors
- Register write protection
- Configurable 1, 2, 4, 8, 16, 32, 64 or 128 Hz square wave output with optional interrupt
- Lock support of register access for control and alarm register

4.5.6 Programmable Trigger Unit (PTU)

- 8 configurable PTU channels for ADC hardware trigger
- Each trigger output can be enabled/disabled independently
- Configurable delay trigger output
- Support bypass of trigger delay
- Support software trigger source
- Support continuous mode
- Optional interrupt of counter and sequence error
- Support pulse out as ACMP's sample window

4.6 Security, Integrity and Safety

4.6.1 Cyclic Redundancy Check (CRC)

- The following CRC polynomials are implemented:
  - CRC4 (CRC-ITU):
    $X^4 + X + 1$
  - CRC16 (CRC-CCITT):
    $X^{16} + X^{12} + X^5 + 1$
  - CRC32 (CRC-ethernet):
    $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable initial seed
- Optional bit-swap in one byte is available for input data
- Optional bit-swap in one word is available for output data
- Optional bit-inversion is available for output data
- 8/16/32-bit access for CRC input data

4.6.2 Hardware Cryptography Unit (HCU)

- Support AES-128 (ECB/CBC/CMAC)
- Support both encryption and decryption
- Support secure hardware key and flexible software key
- All data is in big-endian format
- Support 1-bit, 8-bit and 16-bit data swap
- Size of input/output FIFO is up to 8*32 bits
- Support DMA transport between chip memory and input/output FIFO
- Support several interrupts
  - Operation done interrupt
  - Input FIFO empty interrupt
  - Output FIFO full interrupt
  - Input FIFO overflow interrupt
  - Output FIFO underflow interrupt
  - Input/output FIFO watermark interrupt
- Clock gating strategy is used for engine core when input/output FIFO is not ready

4.6.3 True Random Number Generator (TRNG)

- Generate a 256-bit entropy
- Monobit limit test

- Long run test
- 1 ring OSC with clock checker
- 3 interrupt sources

4.6.4 Watchdog (WDG)

- 32-bit countdown timer
- Functional clock can be selected from IPC and bus clock
- Support regular or window servicing mode
- Support reset request or interrupt for first timeout
- Hard and soft configuration lock bits
- Support fixed key for dog feeding

4.6.5 External Watchdog (EWDG)

- Independent SIRC clock source
- Programmable time-out period
- Windowed refresh option
- Provides robust check that program flow is faster than expected
- Programmable window
- Refresh operation should be done within 63 peripheral bus clock cycles
- An output pad EWDG_OUT_b is used to indicate operation error
- An input pad EWDG_IN is used for external circuit to control EWDG_OUT_b output directly

4.6.6 ECC Management Unit (EMU)

- Two channels to ECC injection and report: TCML and TCMU
- Two-stage enable mechanism to ECC injection and ECC report
- Location and correction or non-correction error can be injected
- ECC error interrupt under each enable register's control
- The last error information can be recorded, including address and syndrome

4.7 Communication Interfaces

4.7.1 Flexible Controller Area Network (FlexCAN)

- Full implementation of the CAN FD protocol and CAN Specification 2.0, Part B
  - Standard data frames
  - Extended data frames
  - Zero to sixty-four bytes data length
  - Programmable bit rate
  - Content-related addressing
- Compliant with the ISO 11898-1 standard
- Silicon-proven implementation passing ISO 16845-1:2016 CAN conformance tests
- Flexible mailboxes configurable to store 0 to 8, 16, 32, or 64 bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Legacy Rx FIFO with storage capacity for up to 6 CAN frames and automatic internal pointer handling with DMA support

- Full-featured Enhanced Rx FIFO with storage capacity for up to 20 CAN FD frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Flexible message buffers, totaling 64 message buffers of 8 bytes data length each, configurable as Rx or Tx
- Programmable clock source to the CAN Protocol Engine, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer with an optional external time tick or high-resolution 32-bit on-chip timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low-power modes, with programmable wakeup on bus activity or matching with received frames (Pretended Networking)
- Transceiver Delay Compensation feature when transmitting CAN FD messages at faster data rates
- Remote request frames may be managed automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to indicate that the FlexCAN is synchronous with CAN bus
- CRC status for transmitted message
- Legacy Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Legacy Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 ID Filter Table elements
- Powerful Enhanced Rx FIFO ID filtering, capable of matching incoming IDs against either 64 extended or 128 standard ID filter elements with three filtering schemes: mask + filter, range, and two filters without mask
- 100% backward compatibility with previous FlexCAN version
- Supports Pretended Networking functionality in low-power modes: Deepsleep mode

4.7.2 Local Interconnect Network (LINFlexD)

- LINFlexD common features in both LIN and UART mode:
  - Support asynchronous functional clock from IPC
  - Fractional baud rate generator
  - Three operating modes for power saving and configuration registers lock
    - Initialization
    - Normal
    - Sleep
  - Test mode: Loop Back
  - Maskable interrupts
- LIN mode features include:
  - Support edge wakeup under low power mode
  - Support for LIN protocol versions 1.3, 2.0, 2.1 and 2.2
  - Bit rates up to 20 Kbit/s (LIN protocol)
  - Master/slave modes

  - Classic and enhanced checksum calculation and check
  - Single 8-byte buffer or FIFO for transmission/reception
  - Timeout management
  - Identifier filters
  - DMA interface
  - Support for 16 identifiers
  - Master mode with autonomous message handling
  - Wakeup event on dominant bit detection
  - True LIN field state machine
  - Advanced LIN error detection
  - Header, response and frame timeout
  - Slave mode
    * Autonomous header handling
    * Autonomous transmit/receive data handling
  - Identifier filters for autonomous message handling in slave mode
  - Separate clock for baud rate calculation
- UART mode features include:
  - Full-duplex communication
  - Separate clock for baud rate calculation
  - 7/8 bits data, parity
  - 1/2/3 stop bits
  - 12-bit + parity reception
  - 4-byte buffer for reception; 4-byte buffer for transmission
  - 12-bit counter for timeout management
  - The maximum baud rate achievable is ipg_baud_clk/4 Mbit/s
  - For bit rate $\leq$ ipg_baud_clk/16 Mbit/s
    * 16 times oversampling
    * 3:1 majority voting
  - For ipg_baud_clk/16 Mbit/s $<$ bit rate $\leq$ ipg_baud_clk/8 Mbit/s
    * Reduced oversampling programmable by software
    * 3:1 majority voting for reduced oversampling of 8 samples per bit
  - For ipg_baud_clk/8 Mbit/s $<$ bit rate $\leq$ ipg_baud_clk/4 Mbit/s
    * Reduced oversampling programmable by software
    * 1:1 voting for all reduced oversampling of 4, 5 and 6 samples per bit

4.7.3 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration
- Configurable frame size
- Transmit/Receive FIFO
- Support single line mode
- Support master and slave mode
- Support Transmit/Receive via DMA

4.7.4 Inter-Integrated Circuit (I2C)

- Support standard, fast, fast plus, high speed and ultra fast mode
- Support 7-bit/10-bit address mode with master and slave
- Support SMBus mode
- Support multi-master arbitration and synchronization

- Support master and slave clock stretching
- Transmit/Receive FIFO (master only)
- Analog and digital filter on both SCL and SDA pins
- Support Transmit/Receive via DMA
- I2C1 doesn't support slave mode

4.7.5 Single Edge Nibble Transmission (SENT)

- Always acts as a receiver
- Support selectable functional clock for message receiving
- Support two channels for different devices
- Support SENT protocol specification J2716 JAN2010
- Support programmable input filter for each channel
- Support configurable receive tick times from 3us to 90µs for each channel
- Support auto compensation for variation in SENT transmit clock up to ±25%
- Support configurable number of data nibbles for each channel
- Support status nibble optionally included in the checksum
- Support pause pulse for each channel
- Support separate channel buffer for storing Fast and Slow Serial Message
- Support FIFO mode to store Fast Message from all channels
- Support DMA to access Fast and Slow Serial Message
- Support time stamp for all receive message
- Support varied interrupts
  - Fast Message receive interrupt
  - Slow Serial Message receive interrupt
  - Channel receive error interrupt
  - FIFO/buffer overflow and underflow interrupt
  - Wake up interrupt (any channel busy to trigger)

4.8 Human Machine Interface

4.8.1 General Purpose Input/Output (GPIO)

- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Input register
- Port Data Direction register
- Digital filter for data inputs
- Inversion for data inputs
- Interrupt and DMA
  - Interrupt flag and enable registers for each pin
  - Support for edge sensitive (rising, falling, both) or level sensitive (low, high)
  - Asynchronous Wake-up in Low-power mode
  - Support for interrupt or DMA request
  - Pin interrupt is functional in all digital pin muxing modes

4.8.2 Port Controller (PCTRL)

- Individual pull control fields with pullup, pulldown, and pull-disable support
- Individual slew rate field supporting fast and slow slew rates

- Individual input passive filter field supporting enable and disable of the individual input passive filter on selected pins
- Individual high drive strength enable on selected pins.
- Individual mux control field supporting analog or pin disabled, GPIO, and up to 6 chip-specific digital functions

5 Ordering Information

The following chips are available for ordering.

Table 1: Ordering table

Product	Memory		Package		IO and ADC channel		Communication
Part number	Flash(KB)	SRAM(KB)	Pin count	Package	GPIOs (Normal)	ADC channels	FlexCAN
YTM32B1MD14G0MLLT	512 KB	64 KB	100	LQFP	87	32	3
YTM32B1MD14G0MLHT	512 KB	64 KB	64	LQFP	56	27	3
YTM32B1MD14G0MLHIT	512 KB	64 KB	64	LQFP	56	27	3

5.1 Part Number Information

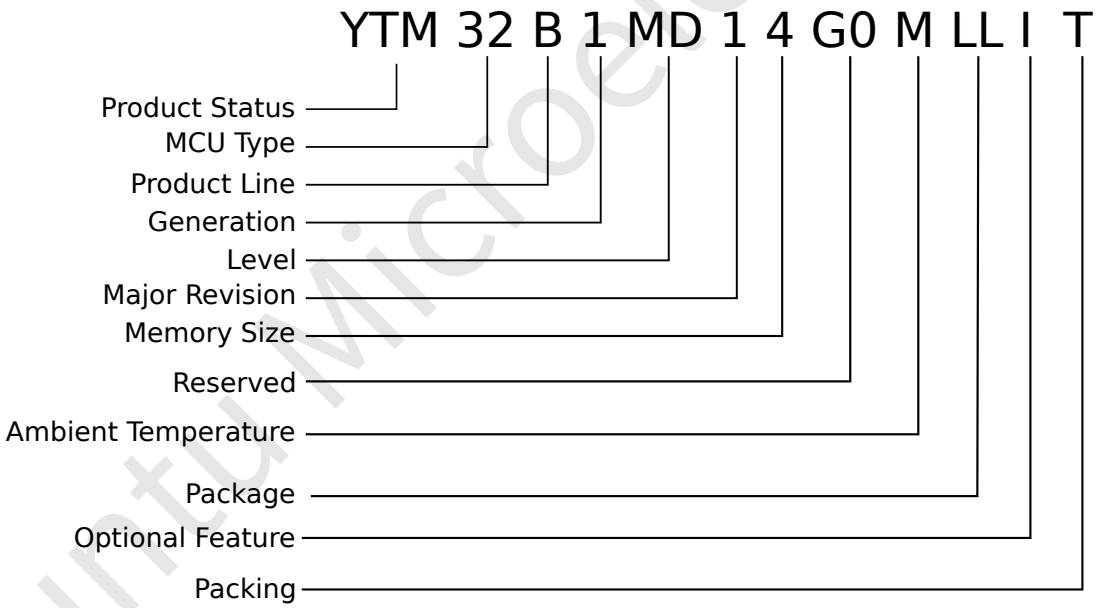


Figure 2: Part Numbers Field

Table 2: Part Number Field Description

Field	Description	Values					
YTM	Product Status	YTM: Qualified PTM: Prototype					
32	MCU Type	32: 32-bit					
B	Product Line	B: General D: Dashboard P: Powertrain V: Vision N: Network					
1	Generation	1st generation product					
MD	Level	Hx: High end Mx: Middle end Lx: Low end					
1	Major Revision	2nd revision					
4	Memory Size		1	2	3	4	5
		H	2M	4M	6M	8M	-
		M	64K	128K	256K	512K	1M
		L	8K	16K	32K	64K	128K
G0	Reserved	Reserved					
M	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C					
LQ	Package	Pins	LQFP	QFN	BGA		
		32	LE	FM	-		
		48	LF	-	-		
		64	LH	-	-		
		100	LL	-	MH		
		144	LQ	-	-		
		176	LU	-	-		
		205	-	-	MK		
		257	-	-	MM		
		289	-	-	MQ		
I	Optional Feature	I: ISELED					
T[1]	Packing	T: Trays/Tubes R: Tape and Reel					

1. The chip mark will not contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ C-Grade\ Part}$	Ambient temperature under bias	-40	–	85	°C
$T_{J\ C-Grade\ Part}$	Junction temperature under bias	-40	–	105	°C
$T_{A\ V-Grade\ Part}$	Ambient temperature under bias	-40	–	105	°C
$T_{J\ V-Grade\ Part}$	Junction temperature under bias	-40	–	125	°C
$T_{A\ M-Grade\ Part}$	Ambient temperature under bias	-40	–	125	°C
$T_{J\ M-Grade\ Part}$	Junction temperature under bias	-40	–	150	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	-500	500	V	
	Corner pins only	-750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	-100	100	mA	3
	Latch-up current at ambient temperature of 25 °C	-200	200	mA	

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

6.2 DC Characteristics

6.2.1 Absolute Maximum Ratings

Table 6: Absolute maximum ratings for YTM32B1MD1x series

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	-0.3	5.8[1]	V	
I_{VDD}	Maximum current into V_{DD}	–	400	mA	
V_{IO}	Digital/Analog IO Input voltage	-0.3	V_{DD} + 0.3	V	
I_O	Instantaneous maximum current of single pin	-25	25	mA	
V_{DDA}	Analog supply voltage	V_{DD} - 0.3	V_{DD} + 0.3	V	

1. 60 seconds lifetime - No restrictions i.e. the part is not held in reset and can switch.

10 hours lifetime - The part is held in reset by an external circuit i.e. the part cannot switch.

NOTE:

- The maximum ratings are the limits to which the device can be subjected without permanently damaging the device.
- The device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

6.2.2 Voltage and Current Operating Requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.97	5.5	V	
V_{DDA}	Analog supply voltage	2.97	5.5	V	
V_{REFH}	Reference voltage	2.97	5.5	V	
$V_{DD} - V_{DDA}$	V_{DD} to V_{DDA} differential voltage	-0.1	0.1	V	
I_{ICIO}	DC injection current - single pin				
	$V_{IN} < V_{SS}$ - 0.3V (Negative current injection)	-3	–	mA	1
	$V_{IN} < V_{SS}$ + 0.3V (Positive current injection)	–	3	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of positive rejection currents of 16 contiguous pins	–	25	mA	

1. All pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{SS} – 0.3V or greater than V_{DD} + 0.3V, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{SS}–0.3V–V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R = [V_{IN}–(V_{DD} + 0.3V)]/|I_{ICIO}|$. The actual resistor values should be an order of magnitude higher to tolerate transient voltages.

6.2.3 DC Electrical Specifications at 3.3V

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	2.97	3.3	4.0	V	
V_{ih}	Input buffer high voltage	0.7 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.3 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	8	–	mA	
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	–	8	–	mA	
I_{oh}	High drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	12	–	mA	
I_{ol}	High drive I/O current sink capability measured when pad = 0.8V	–	12	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin)	–	TBD	–	nA	
V_{OH}	Output high voltage					
	Normal drive pad (2.97V $\leq$ V_{DD} $\leq$ 4.0V, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	–	V	
V_{OL}	Output low voltage					
	Normal drive pad (2.97V $\leq$ V_{DD} $\leq$ 4.0V, I_{OL} = -2.8mA)	–	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	–	0.002	–	μA	
R_{PU}	Internal pull-up resistors	20	–	100	kΩ	
R_{PD}	Internal pull-down resistors	20	–	105	kΩ	

6.2.4 DC Electrical Specifications at 5.0V

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O supply voltage	4	5	5.5	V	
V_{ih}	Input buffer high voltage	0.65 * V_{DD}	–	V_{DD} + 0.3	V	
V_{il}	Input buffer low voltage	V_{SS} - 0.3	–	0.35 * V_{DD}	V	
V_{hys}	Input buffer hysteresis	0.06 * V_{DD}	–	–	V	
I_{oh}	Normal drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	10	–	mA	

Table 9 continued from previous page

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
I_{ol}	Normal drive I/O current sink capability measured when pad = 0.8V	–	10	–	mA	
I_{oh}	Hign drive I/O current source capability measured when pad = (V_{DD} - 0.8V)	–	15	–	mA	
I_{ol}	Hign drive I/O current sink capability measured when pad = 0.8V	–	15	–	mA	
I_{leak}	Hi-Z (Off state) leakage current (per pin)	–	TBD	–	nA	
V_{OH}	Output high voltage					
	Normal drive pad (2.97V $\leq V_{DD} \leq$ 4.0V, I_{OH} = -2.8mA)	V_{DD} - 0.8	–	–	V	
V_{OL}	Output low voltage					
	Normal drive pad (2.97V $\leq V_{DD} \leq$ 4.0V, I_{OL} = -2.8mA)	–	–	0.8	V	
I_{OLT}	Output low current total for all ports	–	–	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	–	0.005	0.5	μA	
R_{PU}	Internal pull-up resistors	20	–	70	kΩ	
R_{PD}	Internal pull-down resistors	20	–	70	kΩ	

6.2.5 Voltage Regulator Electrical Characteristics

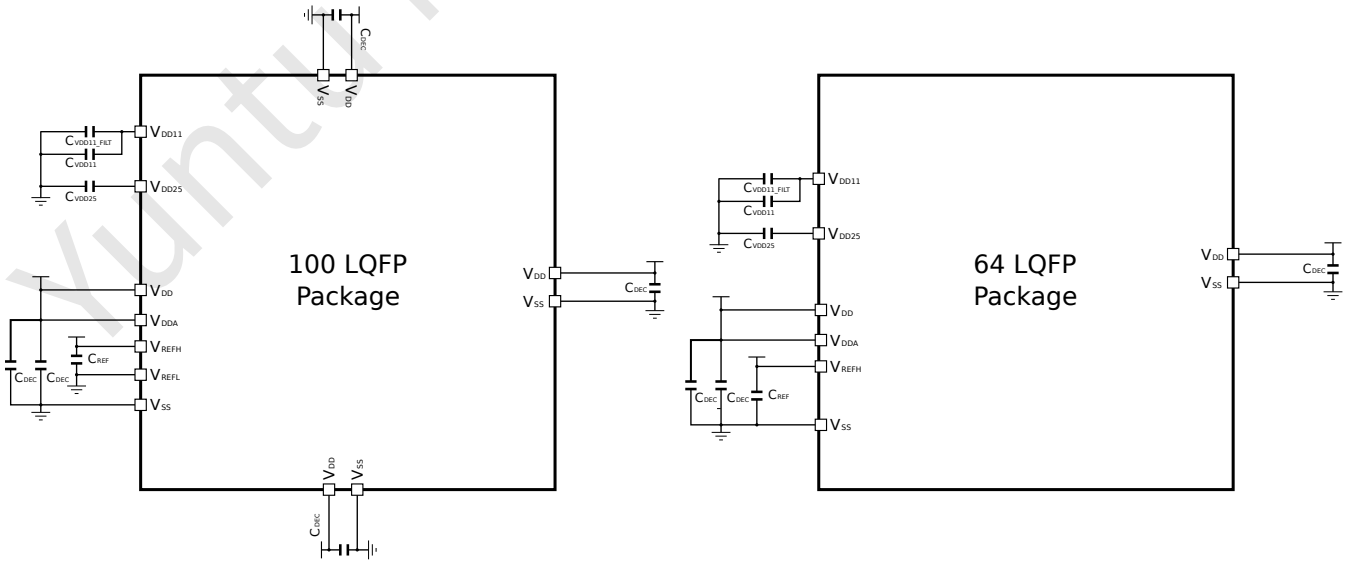


Figure 3: Pinout Decoupling

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF}[1,2]	ADC reference high decoupling capacitance	–	100	–	nF
C_{DEC}[2,3]	Recommended decoupling capacitance	–	100	–	nF
C_{VDD11}	Internal PMC, LDO voltage	–	2.2	–	μF
C_{VDD11_FILT}	Internal PMC, LDO voltage, ripple filter	–	100	–	nF
C_{VDD25}	Internal PMC, LDO voltage	–	220	–	nF

1. For improved ADC performance it is recommended to use 1 nF X7R/C0G and 10 nF X7R ceramics in parallel.
2. The capacitors should be placed as close as possible to the VREFH/VREFL pins or corresponding VDD/VSS pins.
3. The requirement and value of CDEC will be decided by the device application requirement.

6.2.6 POR, LVR and LVD Operating Requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	–	2.0	–	V	
V_{LVD}	Falling low-voltage threshold	2.7	–	2.9	V	
V_{LVD_HYST}	LVD hysteresis	–	20	–	mV	

6.2.7 Power Mode Transition Operating Behaviors

Description	System clock	Frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	FIRC	96MHz	–	800ns	–
SLEEP -> ACTIVE	FXOSC	24MHz	–	TBD	–
SLEEP -> ACTIVE	PLL	120MHz	–	200ns	–
DEEPSLEEP -> ACTIVE	FIRC	96MHz	–	800ns	–
DEEPSLEEP -> ACTIVE	FXOSC	24MHz	–	TBD	–
DEEPSLEEP -> ACTIVE	PLL	120MHz	–	907μs	–
STANDBY -> ACTIVE	FIRC	96MHz	–	800ns	–
STANDBY -> ACTIVE	FXOSC	24MHz	–	900μs	–
STANDBY -> ACTIVE	PLL	120MHz	–	TBD	–
POWERDOWN -> ACTIVE	FIRC	96MHz	–	TBD	–
POWERDOWN -> ACTIVE	FXOSC	24MHz	–	TBD	–
POWERDOWN -> ACTIVE	PLL	120MHz	–	TBD	–
T_{POR}	FIRC(reset value)	96MHz	–	TBD	–

6.2.8 Power Consumption

Mode	Symbol	System clock	Description	Temperature	Min	Typ	Max	Units
ACTIVE	I_{DD_ACTIVE}	FIRC	Running coremark in flash, all peripheral clock enabled. core @96MHz, bus @48MHz V_{DD}=5V	25 °C	–	21.9	–	mA
				125 °C	–	23.7	–	mA
			Running coremark in flash, all peripheral clock disabled. core @96MHz, bus @48MHz V_{DD}=5V	25 °C	–	13.0	–	mA
				125 °C	–	14.6	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @96MHz, bus @48MHz V_{DD}=5V	25 °C	–	20.7	–	mA
				125 °C	–	22.5	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @96MHz, bus @48MHz V_{DD}=5V	25 °C	–	12.0	–	mA
				125 °C	–	13.6	–	mA
		FXOSC	Running coremark in flash, all peripheral clock enabled. core @24MHz, bus @12MHz V_{DD}=5V	25 °C	–	12.2	–	mA
				125 °C	–	14.0	–	mA
			Running coremark in flash, all peripheral clock disabled. core @24MHz, bus @12MHz V_{DD}=5V	25 °C	–	7.6	–	mA
				125 °C	–	9.3	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @24MHz, bus @12MHz V_{DD}=5V	25 °C	–	12.0	–	mA
				125 °C	–	13.7	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @24MHz, bus @12MHz V_{DD}=5V	25 °C	–	7.5	–	mA
				125 °C	–	9.2	–	mA
		PLL	Running coremark in flash, all peripheral clock enabled. core @120MHz V_{DD}=5V	25 °C	–	25.0	–	mA
				125 °C	–	26.8	–	mA
			Running coremark in flash, all peripheral clock disabled. core @120MHz V_{DD}=5V	25 °C	–	14.6	–	mA
				125 °C	–	16.3	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @120MHz V_{DD}=5V	25 °C	–	23.6	–	mA
				125 °C	–	25.4	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @120MHz V_{DD}=5V	25 °C	–	13.4	–	mA
				125 °C	–	15.0	–	mA
			Running while(1) loop in sram, all peripheral clock enabled. core @120MHz V_{DD}=5V	25 °C	–	24.6	–	mA
				125 °C	–	26.6	–	mA
			Running while(1) loop in sram, all peripheral clock disabled. core @120MHz V_{DD}=5V	25 °C	–	14.2	–	mA
				125 °C	–	16.1	–	mA
SLEEP	I_{DD_SLEEP}	PLL	Sleep mode current, V_{DD}=5V Core Frequency @120MHz SIRC enabled	$\leq$ 25 °C	–	9.0	–	mA
				125 °C	–	10.7	–	mA
DEEPSLEEP	$I_{DD\_DEEPSLEEP}$	PLL	Deepsleep mode current, V_{DD}=5V SIRC enabled	$\leq$ 25 °C	–	1.9	–	mA
				125 °C	–	3.5	–	mA
			Deepsleep mode current, V_{DD}=5V SIRC disabled	$\leq$ 25 °C	–	1.9	–	mA
				125 °C	–	3.4	–	mA
STANDBY	$I_{DD\_STANDBY}$	PLL	Standby mode current, V_{DD}=5V SIRC enabled	$\leq$ 25 °C	–	261.4	–	μA
				125 °C	–	1.7	–	mA
			Standby mode current, V_{DD}=5V SIRC disabled	$\leq$ 25 °C	–	185.8	–	μA

Table 13 continued from previous page

Mode	Symbol	System clock	Description	Temperature	Min	Typ	Max	Units
				125 °C	–	1.6	–	mA
POWERDOWN	$I_{DD\_POWERDOWN}$	PLL	Powerdown mode current, V_{DD}=5V SIRC enabled	≤ 25 °C	–	55.9	–	μA
				125 °C	–	250.8	–	μA
			Powerdown mode current, V_{DD}=5V SIRC disabled	≤ 25 °C	–	24.7	–	μA
				125 °C	–	211.3	–	μA

6.2.9 Power Sequence

Hardwares must follow the sequence below to ensure that the chip is powered up properly.

1. VDD must be powered up first.
2. VDDA must be powered up later than or at the same time as VDD.
3. VREFH must be powered up later than or at the same time as VDDA.

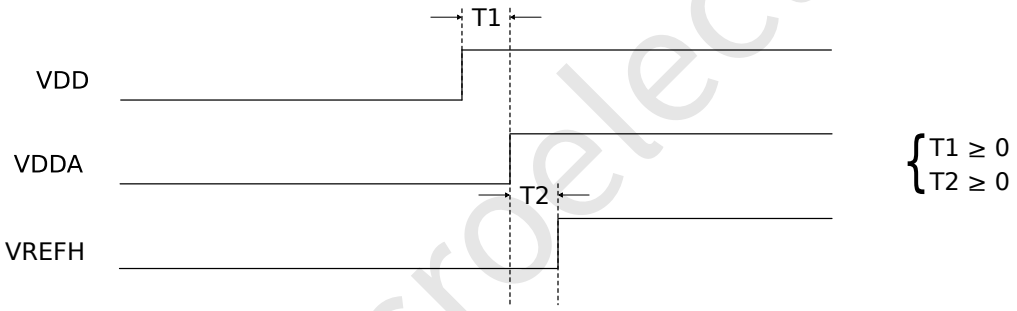


Figure 4: Power Sequence

6.3 AC Characteristics

6.3.1 Device Clock Specifications

Symbol	Description	Min.	Typ.	Unit	Notes
f_{core}	System and core clock	–	120	MHz	
f_{fbus}	Fast bus clock	–	120	MHz	
f_{sbus}	Slow bus clock	–	40	MHz	

6.3.2 I/O Electrical Characteristics

6.3.2.1 AC Electrical Characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and the rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

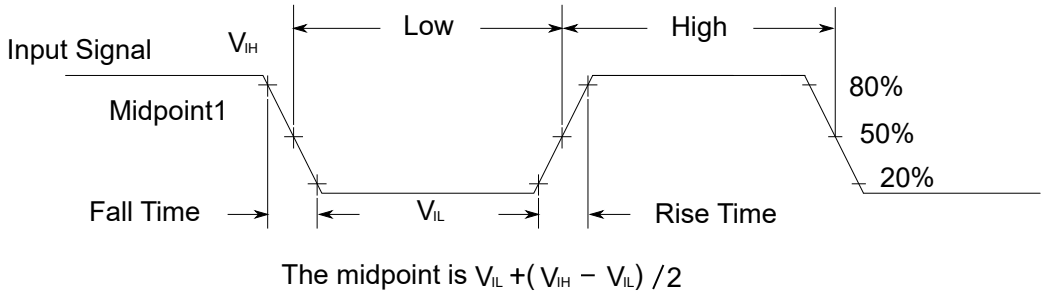


Figure 5: Input Signal Measurement Reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L = 30pF loads
- Normal drive strength

6.4 Peripheral Operating Requirements and Behaviors

6.4.1 FXOSC(4~40 MHz) Characteristics

The following diagram is FXOSC circuit.

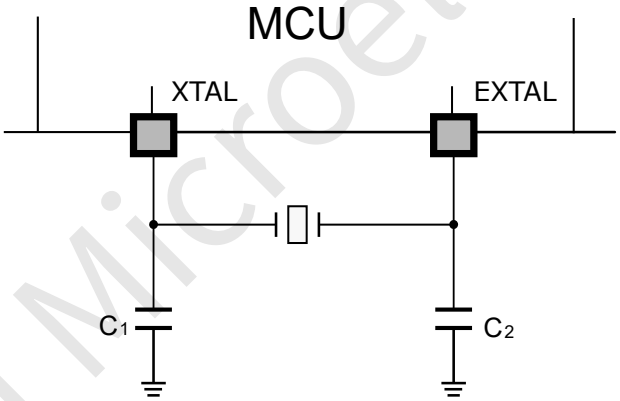


Figure 6: FXOSC Diagram

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDOSC}	FXOSC oscillator (24MHz oscillator)	–	0.4	–	mA	
$T_{FXOSCSU}$	FXOSC startup time (24MHz oscillator)	–	0.5	–	ms	
D_{FXOSC}	Duty of FXOSC (24MHz oscillator)	45	50	55	%	
F_{FXOSC}	FXOSC frequency range	4	–	40	MHz	
C_1	Load capacitance	–	–	–	pF	1
C_2	Load capacitance	–	–	–	pF	
R_F	FXOSC Internal feedback resistor	–	500	–	KΩ	
V_{PP}	Peak-to-peak amplitude of oscillation (24MHz oscillator)	–	2.25	–	V	

1. Depending on the oscillator manual, $C_L = (C_1 * C_2/(C_1 + C_2)) + C_S$. For crystal load balance, $C_1 = C_2$. C_S is parasitic capacitors, C_L is load capacitor of oscillator, calculate C_1 and C_2 according to this formula.

6.4.2 PLL Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{ref}	PLL reference frequency range	8	–	96	MHz	
F_{input}	PLL input frequency	8	–	48	MHz	5
F_{vco}	VCO frequency	200	–	400	MHz	
F_{out}	Out frequency	100	–	200	MHz	1, 4
N_{ref_div}	Reference clock predivider divider	1	–	16		2
N_{fd_div}	VCO feedback divider	10	–	64		3

1. PLL OUT divider is 2, $F_{out} = F_{vco}/2$
2. PLL clock reference divider is from 1 to 16. If need to re-configure. It is recommended to switch to other clock source, then disable PLL, and configure PLL reference divider, switch to PLL, and enable it finally.
3. PLL clock feedback divider is from 10 to 64. It is recommended to switch to other clock source, then disable PLL, and configure PLL reference divider, switch to PLL, and enable it finally.
4. $F_{out} = \frac{F_{ref}}{2*N_{ref\_div}} * N_{fb\_div}$
5. $F_{input} = \frac{F_{ref}}{N_{ref\_div}}$

6.4.3 FIRC(96 MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{FIRC}	Fast internal reference frequency	–	96	–	MHz	
ACC_{FIRC}	FIRC frequency accuracy, factory trimmed and temperature $\leq$ 25 °C	-1.0	–	1.0	%	
	FIRC frequency accuracy, factory trimmed and temperature $\leq$ 125 °C	-1.5	–	1.5	%	
I_{FIRC}	FIRC operating current	–	770	–	μA	
$T_{Startup}$	Startup time	–	3	–	μs	

6.4.4 SIRC(12 MHz) Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{SIRC}	Slow internal reference frequency	–	12	–	MHz	
ACC_{SIRC}	SIRC frequency accuracy, factory trimmed and temperature $\leq$ 25 °C	-1.0	–	1.0	%	

Table 18 continued from previous page

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	SIRC frequency accuracy, factory trimmed and temperature $\leq$ 125 °C	-6.0	–	6.0	%	
I_{SIRC}	SIRC operating current	–	16	–	μA	
$T_{Startup}$	Startup time	–	10	–	μs	

6.4.5 ADC Characteristics

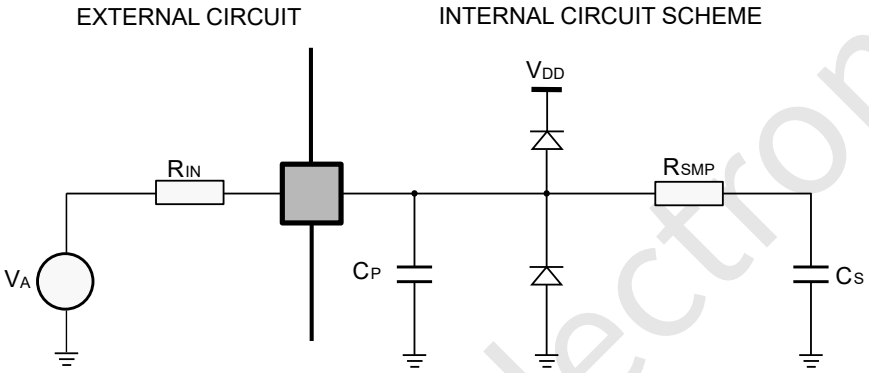


Figure 7: ADC Circuit

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{DDA}	Analog supply voltage		2.97	5.0	5.5	V	
I_{DDA}	Analog supply current		–	TBD	–	mA	
ΔV_{DDA}	V_{DD} - V_{DDA}		-100	–	100	mV	
V_{REFH}	Reference voltage		2.97	–	V_{DDA}	V	
I_{REFH}	Reference current		–	TBD	–	μA	
V_{IN}	Input voltage		0	–	V_{REFH}	V	
R_{SMP}	Sampling switch impedance		0.18	0.64	1.5	kΩ	
R_{IN}	Input impedance	Sample rate is 1MHz	–	150	–	kΩ	
C_P	Pin Capacitance		–	3	–	pF	
C_S	Sampling capacitance		–	6.5	–	pF	

Symbol	Description	Test condition[1]	Min.	Typ.	Max.	Unit	Notes
$T_{STARTUP}$	Analog startup time		–	2	–	μs	
T_{SAMPLE}	Sampling time	ADC functional clock is 32MHz	4	–	–	cycles	

Table 20 continued from previous page

Symbol	Description	Test condition[1]	Min.	Typ.	Max.	Unit	Notes
T_{CONV_12BIT}	Total conversion time with sample	ADC functional clock is 32MHz and select 12-bit resolution	–	16	–	cycles	
T_{CONV_10BIT}	Total conversion time with sample	ADC functional clock is 32MHz and select 10-bit resolution	–	14	–	cycles	
T_{CONV_8BIT}	Total conversion time with sample	ADC functional clock is 32MHz and select 8-bit resolution	–	12	–	cycles	
T_{CONV_6BIT}	Total conversion time with sample	ADC functional clock is 32MHz and select 6-bit resolution	–	10	–	cycles	

1. Theses parameters of this table can be configured by register, please refer to Reference Manual for details.

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
E_{GAIN}	Gain error	12-bit resolution	–	TBD	–	LSB	
E_{OFFSET}	Offset error	12-bit resolution	–	TBD	–	LSB	
ENOB	Effective number bits	12-bit resolution	–	10.5	–	Bits	
SINAD	Signal-to-noise-and-distortion ratio	12-bit resolution	–	TBD	TBD	dB	

6.4.6 ACMP Characteristics

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit	Notes
V_{ACMP}[1]	Analog supply voltage		2.97	5.0	5.5	V	
I_{ACMP}	Analog supply current		–	TBD	–	μA	
$V_{INOFFSET}$	Analog input offset voltage		TBD	–	TBD	mV	
V_{IN}	Analog input voltage		0	–	V_{ACMP}	V	
V_{HYST0}	Analog comparator hysteresis 0		–	TBD	–	mV	
V_{HYST1}	Analog comparator hysteresis 1		–	TBD	–	mV	

1. This connects to VDD.

6.4.7 NVM Specifications

6.4.7.1 Flash Timing Specifications - Commands

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T_{pgm}	Program execution time	–	45	47	μs	
T_{sector_erase}	Sector erase execution time	–	16	–	ms	
T_{block_erase}	Block erase execution time	–	16	–	ms	
T_{chip_erase}	Chip erase execution time	–	16	–	ms	
T_{erase_retry}	Erase retry execution time	–	1	16	ms	

6.4.7.2 Reliability Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{nvmretp}$	Data retention	20	–	–	years	
$t_{nvmcycp}$	Cycling endurance	100,000	–	–	cycles	

6.4.8 Debug Module Electrical

6.4.8.1 SWD Electrical Specifications

Table 25: SWD full voltage range electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

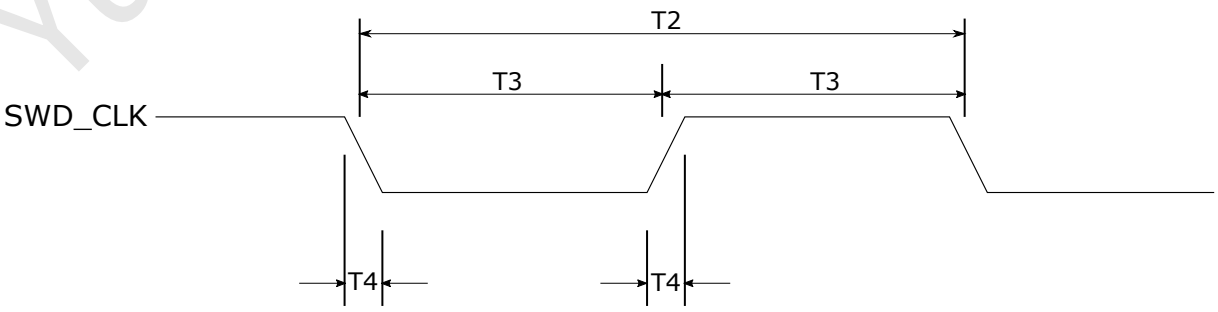


Figure 8: SWD Clock Timing

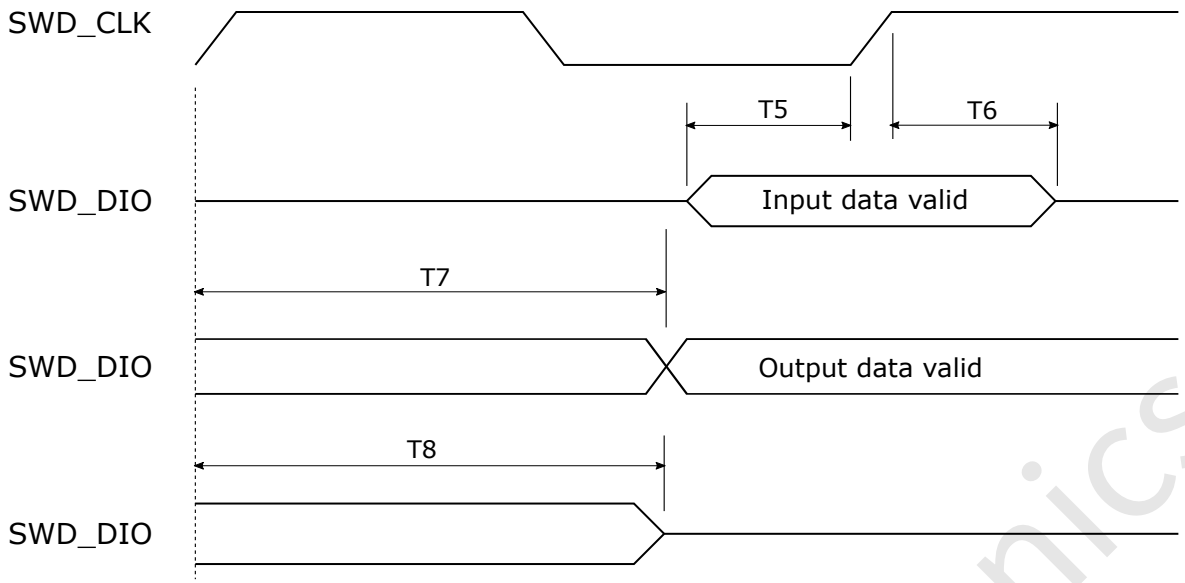


Figure 9: SWD Data Timing

6.4.8.2 JTAG Electrical Specifications

Table 26: JTAG Electrical Specifications

Symbol	Description	Active				Unit
		5.0V IO		3.3V IO		
		Min.	Max.	Min.	Max.	
J1	TCLK frequency					MHz
	Boundary Scan	–	20	–	20	
	JTAG	–	20	–	20	
J2	TCLK cycle period	1/J1	–	1/J1	–	ns
J3	TCLK clock pulse width					ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG					
J4	TCLK rise and fall times	–	1	–	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	–	5	–	ns
J6	Boundary scan input data hold time after TCLK rise	5	–	5	–	ns
J7	TCLK low to boundary scan output data valid	–	28	–	32	ns
J8	TCLK low to boundary scan output data invalid	0	–	0	–	ns
J9	TCLK low to boundary scan output high-Z	–	28	–	32	ns
J10	TMS, TDI input data setup time to TCLK rise	3	–	3	–	ns
J11	TMS, TDI input data hold time after TCLK rise	2	–	2	–	ns
J12	TCLK low to TDO data valid	–	28	–	32	ns
J13	TCLK low to TDO data invalid	0	–	0	–	ns
J14	TCLK low to TDO high-Z	–	28	–	28	ns

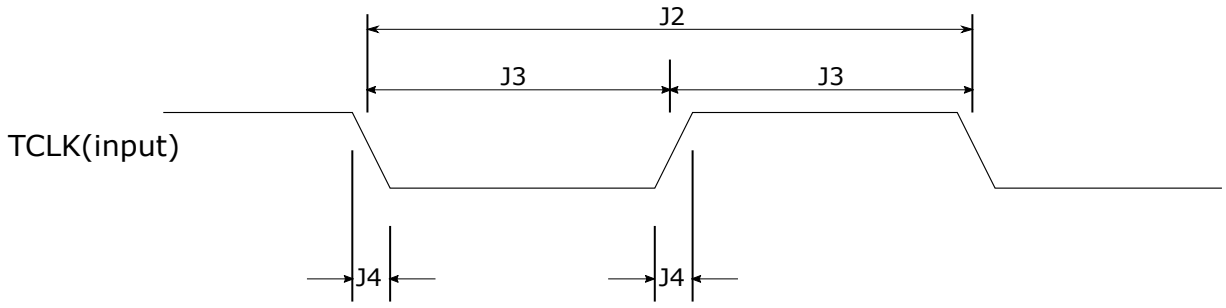


Figure 10: JTAG Clock Timing

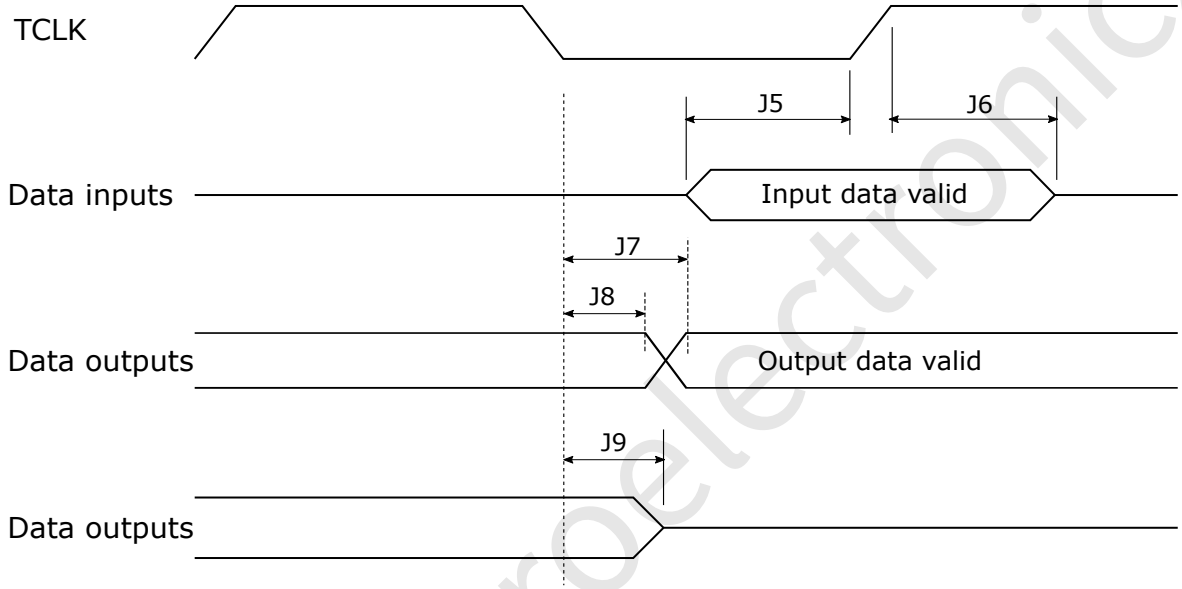


Figure 11: JTAG Data Timing

6.5 Thermal Attributes

Table 27: Thermal Characteristics

Package Family	Package Type	Thermal Resistance JA (°C/W)
LQFP	LQFP64L	65
	LQFP100L	57

7 Pinouts

7.1 IO Signal Description

The pinouts signal description is as follows:

Table 28: Pinmux Table

100 LQFP	64 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	-	PTE_16	-	PTE_16	-	SPI2_SIN	eTMR2_CH7	-	-	TMU_OUT7
2	-	PTE_15	-	PTE_15	-	SPI2_SCK	eTMR2_CH6	-	-	TMU_OUT6
3	1	VDD11	VDD11	-	-	-	-	-	-	-
4	2	VDD25	VDD25	-	-	-	-	-	-	-
5	3	PTE_11	-	PTE_11	SPI2_PCS0	lpTMR0_ALT1	eTMR2_CH5	SENT_RX_IN1	ETM_TRACE_D0	TMU_OUT5
6	4	PTE_10	-	PTE_10	SCU_CLKOUT	SPI2_PCS1	eTMR2_CH4	-	-	TMU_OUT4
7	-	PTE_13	-	PTE_13	-	SPI2_PCS2	eTMR2_FLT0	-	-	-
8	5	PTE_5	-	PTE_5	TCLK_IN2	eTMR2_QD_PHA	eTMR2_CH3	CAN0_TX	-	EWDG_IN
9	6	PTE_4	-	PTE_4	ETM_TRACE_D1	eTMR2_QD_PHB	eTMR2_CH2	CAN0_RX	-	EWDG_OUT_b
10	7	VDD	VDD	-	-	-	-	-	-	-
11	8	VDDA	VDDA	-	-	-	-	-	-	-
12	9	VREFH	VREFH	-	-	-	-	-	-	-
13	-	VREFL	VREFL	-	-	-	-		-	-
14	10	VSS	VSS	-	-	-	-	-	-	-
15	11	PTB_7	EXTAL	PTB_7	I2C0_SCL	-	SPI3_SCK	-	-	TMU_OUT2
16	12	PTB_6	XTAL	PTB_6	I2C0_SDA	-	SPI3_SIN	-	-	TMU_OUT1
17	-	PTE_14	-	PTE_14	eTMR0_FLT1	-	eTMR2_FLT1	-	-	-
18	13	PTE_3	-	PTE_3	eTMR0_FLT0	SPI1_SIN	eTMR2_FLT0	SPI3_SOUT	TMU_IN6	ACMP0_OUT
19	-	PTE_12	-	PTE_12	eTMR0_FLT3	LINFlexD2_TX	-	SPI3_PCS0	-	-
20	-	PTD_17	-	PTD_17	eTMR0_FLT2	LINFlexD2_RX	-	-	-	-
21	14	PTD_16	-	PTD_16	eTMR0_CH1	-	SPI0_SIN	ACMP0_ACTIVE	ETM_TRACE_D2	ETM_TRACE_CLKOUT
22	15	PTD_15	-	PTD_15	eTMR0_CH0	-	SPI0_SCK	-	ETM_TRACE_D3	-
23	16	PTE_9	-	PTE_9	eTMR0_CH7	SPI1_SCK	-	-	-	-
24	-	PTD_14	-	PTD_14	eTMR2_CH5	LINFlexD1_TX	-	-	-	SCU_CLKOUT
25	-	PTD_13	-	PTD_13	eTMR2_CH4	LINFlexD1_RX	-	-	-	RTC_CLKOUT
26	17	PTE_8	ACMP0_IN3	PTE_8	eTMR0_CH6	-	-	SPI3_PCS1	-	-
27	18	PTB_5	-	PTB_5	eTMR0_CH5	SPI0_PCS1	SPI0_PCS0	SCU_CLKOUT	TMU_IN0	-
28	19	PTB_4	-	PTB_4	eTMR0_CH4	SPI0_SOUT	-	-	TMU_IN1	-
29	20	PTC_3	ADC0_SE11 ACMP0_IN4	PTC_3	eTMR0_CH3	CAN0_TX	LINFlexD0_TX	-	-	-
30	21	PTC_2	ADC0_SE10 ACMP0_IN5	PTC_2	eTMR0_CH2	CAN0_RX	LINFlexD0_RX	-	ETM_TRACE_CLKOUT	-
31	22	PTD_7	ACMP0_IN6	PTD_7	LINFlexD2_TX	eTMR0_CH3	eTMR2_FLT3	-	ETM_TRACE_D0	-
32	23	PTD_6	ACMP0_IN7	PTD_6	LINFlexD2_RX	eTMR0_CH2	eTMR2_FLT2	-	-	-
33	24	PTD_5	-	PTD_5	eTMR2_CH3	lpTMR0_ALT2	eTMR2_FLT1	-	TMU_IN7	-
34	-	PTD_12	-	PTD_12	eTMR2_CH2	-	ETM_TRACE_D1	-	SPI3_PCS2	-
35	-	PTD_11	-	PTD_11	eTMR2_CH1	eTMR2_QD_PHA	ETM_TRACE_D2	-	SPI3_PCS3	-
36	-	PTD_10	-	PTD_10	eTMR2_CH0	eTMR2_QD_PHB	ETM_TRACE_D3	-	SCU_CLKOUT	-
37	-	VSS	VSS	-	-	-	-	-	-	-
38	-	VDD	VDD	-	-	-	-	-	-	-
39	25	PTC_1	ADC0_SE9	PTC_1	eTMR0_CH1	SPI2_SOUT	-	-	eTMR1_CH7	-
40	26	PTC_0	ADC0_SE8	PTC_0	eTMR0_CH0	SPI2_SIN	-	-	eTMR1_CH6	-
41	-	PTD_9	-	PTD_9	-	-	eTMR2_FLT3	-	eTMR1_CH5	-
42	-	PTD_8	-	PTD_8	-	-	eTMR2_FLT2	-	eTMR1_CH4	-
43	27	PTC_17	ADC0_SE15	PTC_17	eTMR1_FLT3	CAN2_TX	-	eTMR2_CH1	-	-
44	28	PTC_16	ADC0_SE14	PTC_16	eTMR1_FLT2	CAN2_RX	-	eTMR2_CH0	-	-
45	29	PTC_15	ADC0_SE13	PTC_15	eTMR1_CH3	SPI2_SCK	-	-	TMU_IN8	-
46	30	PTC_14	ADC0_SE12	PTC_14	eTMR1_CH2	SPI2_PCS0	-	-	TMU_IN9	-
47	31	PTB_3	ADC0_SE7	PTB_3	eTMR1_CH1	SPI0_SIN	eTMR1_QD_PHA	-	TMU_IN2	-
48	32	PTB_2	ADC0_SE6	PTB_2	eTMR1_CH0	SPI0_SCK	eTMR1_QD_PHB	-	TMU_IN3	-
49	-	PTC_13	-	PTC_13	eTMR3_CH7	eTMR2_CH7	-	-	-	-
50	-	PTC_12	-	PTC_12	eTMR3_CH6	eTMR2_CH6	-	-	-	-

100 LQFP	64 LQFP	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
51	-	PTC_11	-	PTC_11	eTMR3_CH5	-	-	-	TMU_IN10	-
52	-	PTC_10	-	PTC_10	eTMR3_CH4	-	-	-	TMU_IN11	-
53	33	PTB_1	ADC0_SE5	PTB_1	LINFlexD0_TX	SPI0_SOUT	TCLK_IN0	CAN0_TX	-	-
54	34	PTB_0	ADC0_SE4	PTB_0	LINFlexD0_RX	SPI0_PCS0	lpTMR0_ALT3	CAN0_RX	-	-
55	35	PTC_9	-	PTC_9	LINFlexD1_TX	eTMR1_FLT1	-	-	-	-
56	36	PTC_8	-	PTC_8	LINFlexD1_RX	eTMR1_FLT0	-	-	-	-
57	37	PTA_7	ADC0_SE3	PTA_7	eTMR0_FLT2	-	RTC_CLKIN	SENT_RX_IN0	-	-
58	38	PTA_6	ADC0_SE2	PTA_6	eTMR0_FLT1	SPI1_PCS1	-	SENT_RX_IN1	-	-
59	39	PTE_7	-	PTE_7	eTMR0_CH7	eTMR3_FLT0	-	-	-	-
60	40	VSS	VSS	-	-	-	-	-	-	-
61	41	VDD	VDD	-	-	-	-	-	-	-
62	-	PTA_17	-	PTA_17	eTMR0_CH6	eTMR3_FLT0	EWDG_OUT_b	-	-	-
63	-	PTB_17	-	PTB_17	eTMR0_CH5	SPI1_PCS3	-	-	-	-
64	-	PTB_16	ADC0_SE31	PTB_16	eTMR0_CH4	SPI1_SOUT	-	-	-	-
65	-	PTB_15	ADC0_SE30	PTB_15	eTMR0_CH3	SPI1_SIN	-	-	-	-
66	-	PTB_14	ADC0_SE25	PTB_14	eTMR0_CH2	SPI1_SCK	-	-	-	-
67	42	PTB_13	ADC0_SE24	PTB_13	eTMR0_CH1	eTMR3_FLT1	CAN2_TX	SPI3_PCS2	-	-
68	43	PTB_12	ADC0_SE23	PTB_12	eTMR0_CH0	eTMR3_FLT2	CAN2_RX	SPI3_PCS3	-	-
69	44	PTD_4	ADC0_SE22	PTD_4	eTMR0_FLT3	eTMR3_FLT3	-	-	-	-
70	45	PTD_3	ADC0_SE19	PTD_3	eTMR3_CH5	SPI1_PCS0	I2C1_SCL	-	TMU_IN4	NMI_b
71	46	PTD_2	ADC0_SE18	PTD_2	eTMR3_CH4	SPI1_SOUT	I2C1_SDA	-	TMU_IN5	-
72	47	PTA_3	ADC0_SE17	PTA_3	eTMR3_CH1	I2C0_SCL	EWDG_IN	SENT_RX_IN0	LINFlexD0_TX	-
73	48	PTA_2	ADC0_SE16	PTA_2	eTMR3_CH0	I2C0_SDA	EWDG_OUT_b	SENT_RX_IN1	LINFlexD0_RX	-
74	-	PTB_11	-	PTB_11	eTMR3_CH3	-	-	-	-	-
75	-	PTB_10	-	PTB_10	eTMR3_CH2	-	-	-	-	-
76	-	PTB_9	-	PTB_9	eTMR3_CH1	-	-	-	-	-
77	-	PTB_8	-	PTB_8	eTMR3_CH0	-	-	-	-	-
78	49	PTA_1	ADC0_SE1 ACMP0_IN1	PTA_1	eTMR1_CH1	-	-	eTMR1_QD_PHA	-	TMU_OUT0
79	50	PTA_0	ADC0_SE0 ACMP0_IN0	PTA_0	eTMR2_CH1	-	-	eTMR2_QD_PHA	-	TMU_OUT3
80	51	PTC_7	ADC0_SE21	PTC_7	LINFlexD1_TX	CAN1_TX	eTMR3_CH3	-	eTMR1_QD_PHA	-
81	52	PTC_6	ADC0_SE20	PTC_6	LINFlexD1_RX	CAN1_RX	eTMR3_CH2	-	eTMR1_QD_PHB	-
82	-	PTA_16	ADC0_SE29	PTA_16	eTMR1_CH3	SPI1_PCS2	-	-	-	-
83	-	PTA_15	ADC0_SE28	PTA_15	eTMR1_CH2	SPI0_PCS3	SPI2_PCS3	-	-	-
84	53	PTE_6	ADC0_SE27	PTE_6	SPI0_PCS2	-	eTMR3_CH7	SENT_RX_IN1	ETM_TRACE_D2	ETM_TRACE_CLKOUT
85	54	PTE_2	ADC0_SE26	PTE_2	SPI0_SOUT	lpTMR0_ALT3	eTMR3_CH6	-	ETM_TRACE_D3	-
86	-	VSS	VSS	-	-	-	-	-	-	-
87	-	VDD	VDD	-	-	-	-	-	-	-
88	-	PTA_14	-	PTA_14	eTMR0_FLT0	eTMR3_FLT1	EWDG_IN	-	eTMR1_FLT0	-
89	55	PTA_13	-	PTA_13	eTMR1_CH7	CAN1_TX	SPI3_PCS0	-	eTMR2_QD_PHA	-
90	56	PTA_12	-	PTA_12	eTMR1_CH6	CAN1_RX	SPI3_SCK	-	eTMR2_QD_PHB	-
91	57	PTA_11	-	PTA_11	eTMR1_CH5	-	SPI3_SIN	ACMP0_ACTIVE	-	-
92	58	PTA_10	-	PTA_10	eTMR1_CH4	-	SPI3_SOUT	-	-	JTAG_TDO SWD_SWO
93	59	PTE_1	-	PTE_1	SPI0_SIN	-	SENT_RX_IN0	SPI1_PCS0	eTMR1_FLT1	-
94	60	PTE_0	-	PTE_0	SPI0_SCK	TCLK_IN1	-	SPI1_SOUT	eTMR1_FLT2	-
95	61	PTC_5	-	PTC_5	eTMR2_CH0	RTC_CLKOUT	SPI3_PCS1	-	eTMR2_QD_PHB	JTAG_TDI
96	62	PTC_4	ACMP0_IN2	PTC_4	eTMR1_CH0	RTC_CLKOUT	-	EWDG_IN	eTMR1_QD_PHB	JTAG_TCK SWD_CLK
97	63	PTA_5	-	PTA_5	-	TCLK_IN1	-	-	-	RESET_b
98	64	PTA_4	-	PTA_4	-	-	ACMP0_OUT	EWDG_OUT_b	-	JTAG_TMS SWD_IO
99	-	PTA_9	-	PTA_9	LINFlexD2_TX	SPI2_PCS0	-	eTMR3_FLT2	eTMR1_FLT3	-
100	-	PTA_8	-	PTA_8	LINFlexD2_RX	SPI2_SOUT	-	eTMR3_FLT3	-	-

7.2 Packages

The information of package pinouts is as follows:

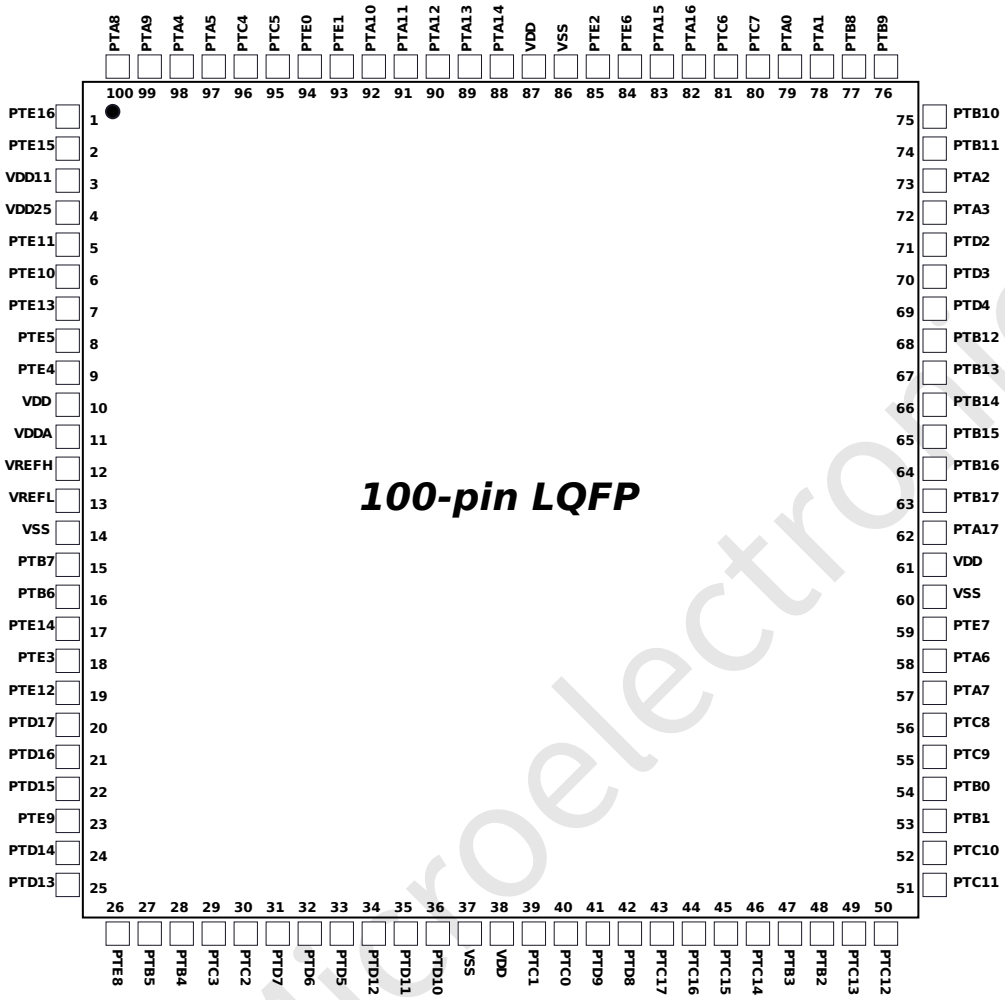


Figure 12: 100-pin LQFP Package

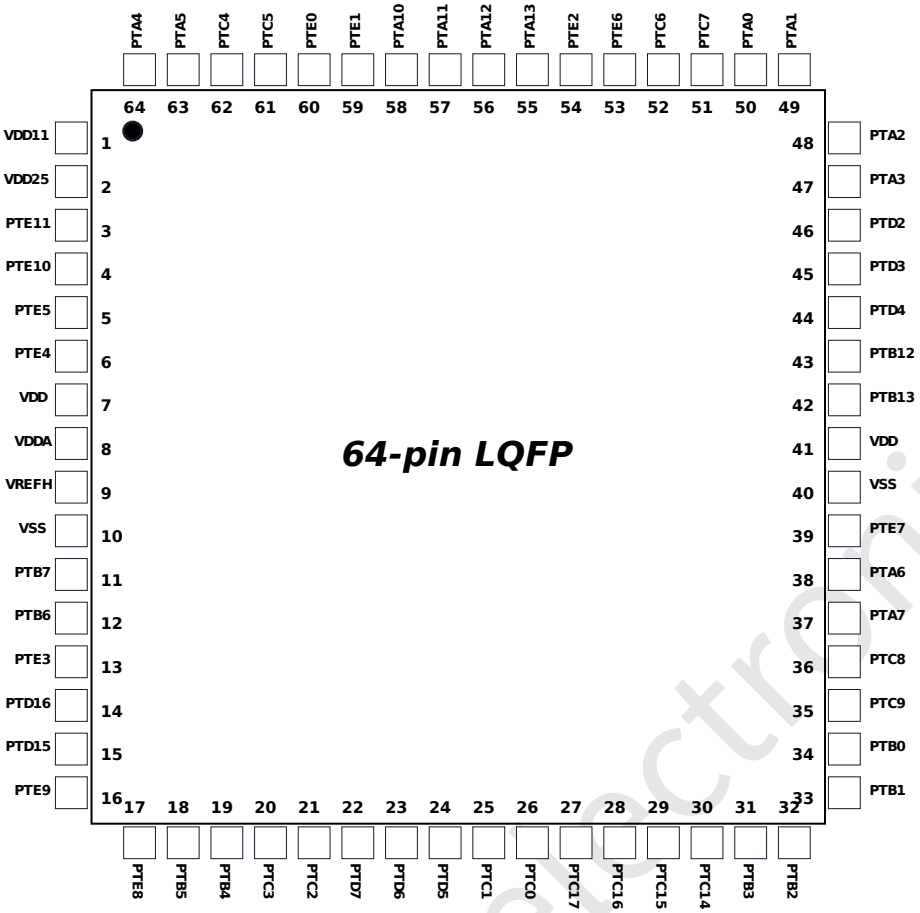
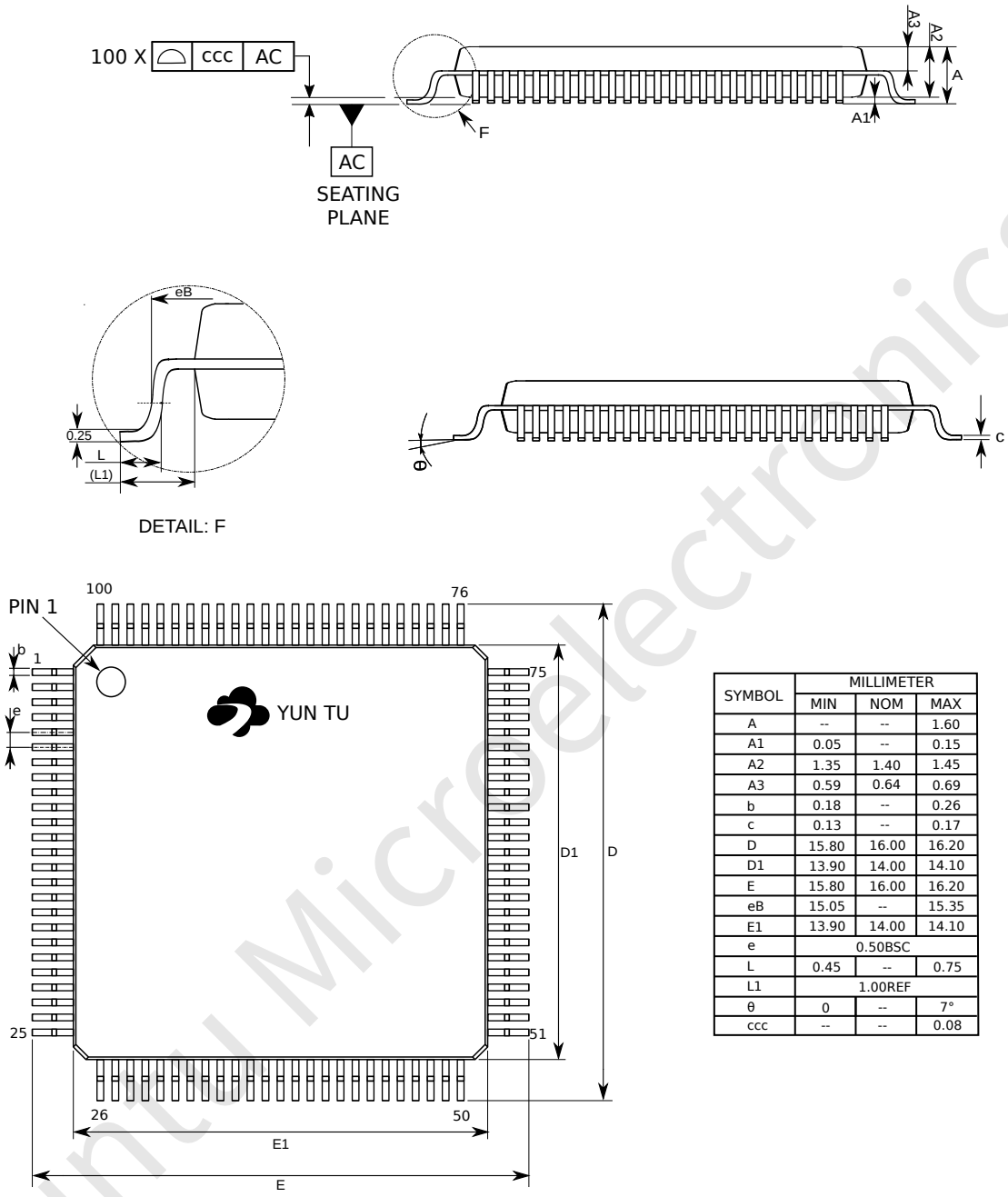


Figure 13: 64-pin LQFP Package

Note: The chip mark will not contain packing information(T/R)

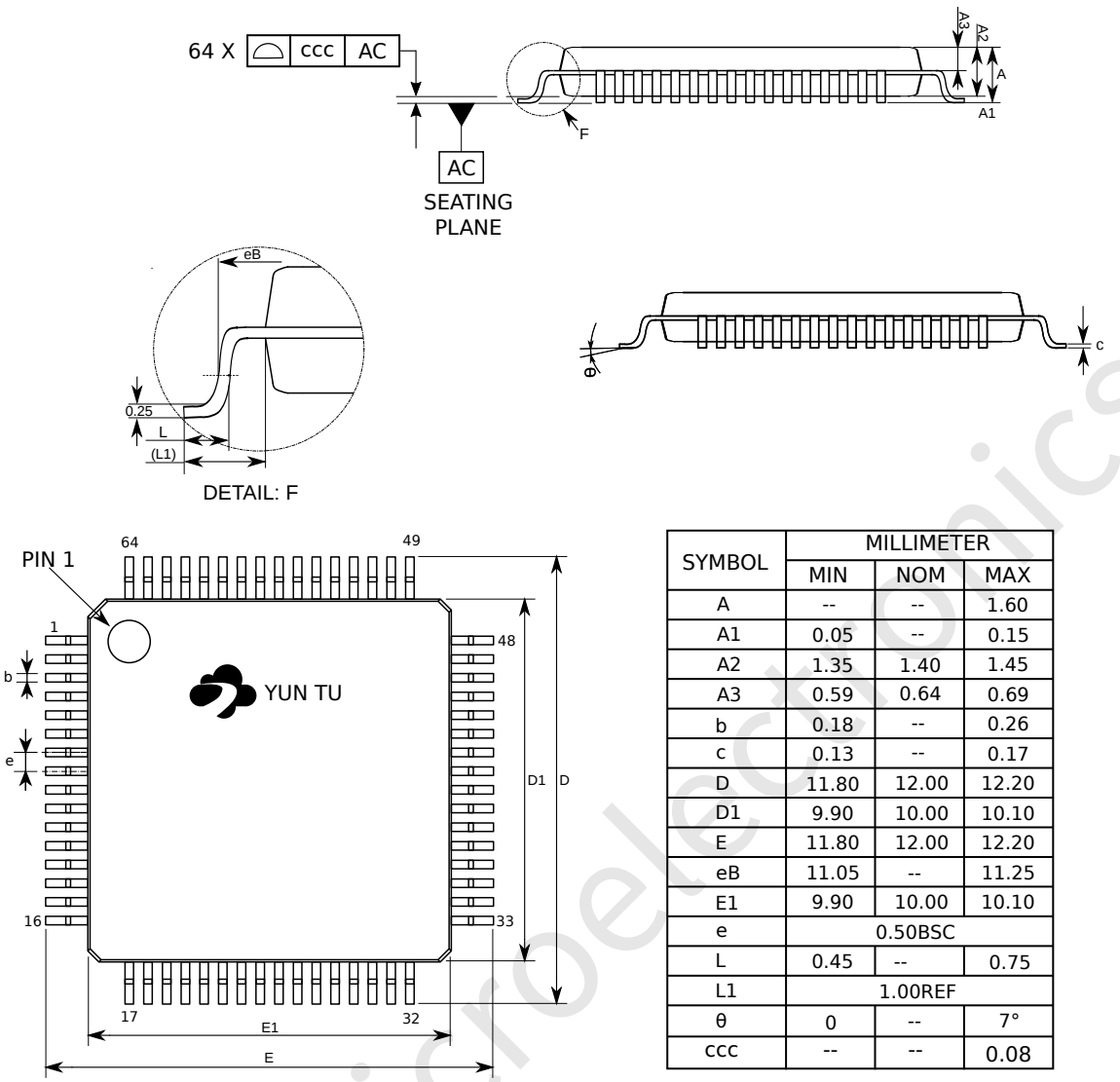
7.3 Dimensions

Package dimensions are as follows:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
c	0.13	--	0.17
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
eB	15.05	--	15.35
E1	13.90	14.00	14.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°
ccc	--	--	0.08

Figure 14: 100-pin LQFP



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	--	0.26
c	0.13	--	0.17
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.05	--	11.25
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		
θ	0	--	7°
ccc	--	--	0.08

Figure 15: 64-pin LQFP

Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2022/7/15	Initial version
1.1	2020/10/25	Added “4 module interrupts” in the chapter of Features Added the number of channels of ADC and ACMP in the chapter of Features Removed the section of Features in the chapter of Overview Added the subsection of Power Sequence Updated some data in the chapter of Electrical Characteristics Added High drive I/O current in the subsection of DC Electrical Specification at 3.3V Added High drive I/O current in the subsection of DC Electrical Specification at 5.0V Added missed VDD in Figure3
1.2	2023/3/06	Removed the DNL and INL in the subsection of ADC Characteristics Added the new section of Thermal Characteristics
1.3	2023/3/13	Added “AEC-Q100 qualified” in Features Summary Added the new chapter of Features Corrected the symbol of Thermal Operating Characteristics Corrected V_{LAT} to I_{LAT} in ESD Handling Ratings
1.4	2023/4/28	Added the information on ASIL B in “Features Summary” and “Overview” Added the support for ISELED in “Part Number Information” Updated the contents in “Absolute Maximum Ratings” Updated the contents in “Voltage and Current Operating Requirements” Updated the values in “DC Electrical Specifications at 3.3V” Updated the contents in “Power Consumption” Corrected the value of Max. to Typ. in “Device Clock Specifications” Added one note in “ADC Characteristics” Updated the contents of “ACMP Characteristics” Removed the unnecessary contents in “Thermal Attributes”
1.5	2023/6/28	Added the coplanarity specifications of product in the section of “Dimensions” Added the location information of PIN 1 in the section of “Dimensions”

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