YTM32Z1MC0x Data Sheet

Support: YTM32Z1MC03X0WFMST, YTM32Z1MC03X0WFMDT

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1 Features Summary

- AEC-Q100 qualified
- ARM Cortex-M0+
  - 32-bit core, running up to 48 MHz
  - Configurable Nested Vectored Interrupt Controller(NVIC)
  - Two-stage pipeline: Reduced number of Cycles Per Instruction(CPI), enabling faster branch instruction and ISR entry, and reducing power consumption
  - Excellent code density to reduced flash size, system cost and power consumption
  - 100 percent compatible with ARM Cortex-M0 and a subset ARM Cortex-M3/M4: Reuse existing compilers and debug tools
  - Simplified architecture: 56 instructions and 17 registers enable easy programming and efficient packaging of 8/16/32-bit data in memory
  - ARM third-party ecosystem support: Software and tools to help minimize development time/cost
  - DIVSQRT module with 32-bit integer divide and square root arithmetic operations
- Memory
  - Up to 32KB Program Flash with ECC, supporting Single Error Correction(SEC) and Double Error Detection(DED)
  - Up to 192B EEPROM with embedded SRAM and NVM(Non-Volatile Memory)
  - Up to 16KB ROM, supporting bootloader with LIN and embedded motor control algorithm
  - Up to 4KB SRAM with ECC, supporting Single Error Correction(SEC) and Double Error Detection(DED)
- Clocks
  - PLL clock, up to 48MHz
  - Internal RC oscillator, up to 2MHz
  - Low power oscillator, run at 10KHz
- Power management
  - Low power ARM Cortex-M0+ with excellent energy efficiency
  - Support four power modes
    - Active
    - Sleep
    - Deepsleep
    - Powerdown
  - Support clock gating for unused modules, and specific peripherals remain working in Sleep, Deepsleep and Powerdown mode
  - Three Powerdown wakeup sources: LIN, internal wakeup timer and external pin(PTA3)
- Analog mixed signal
  - HV LDO: 1.8V LDO for digital and 3.3V LDO for analog
  - One 10-bit, 1Msps Analog-to-Digital Converter(ADC), which has 24 channels, and 0.75V/1.5V/2.5V internal reference
  - One Analog Comparator used for zero-crossing detection in motor driver application
  - On-chip temperature sensor with +/-10°C accuracy
  - Pre-driver
    - One chargepump for highside gate driver and one capless LDO for lowside gate driver
    - Up to four phase pre-driver for small NFETs(<30nC@25kHz PWM) to drive 2x DC, BLDC or Stepper motor
    - Over-current protection
    - Over-voltage and under-voltage protection
    - Over-temperature protection
    - Zero-crossing Detection Unit(ZDU)
- Communications
  - Up to two Universal Asynchronous Receiver Transmitters(UARTs)
  - One Serial Port Interface(SPI)
  - One LIN supports LIN 2.x/SAE J2602
- Timer
  - Periodic Timer(pTMR)
  - Capture and Compare Timer(CCTMR * 2): 2 * 2 channels
  - Motor Specific Pulse Width Modulation(MSPWM) for a broad range of applications including motor control
- Safety
  - Internal Watchdog(WDG) with independent clock source
- Up to 9 GPIO pins with interrupt functionality
  - 7 normal GPIOs support 3.3V operation voltage for communications
  - 1 GPIO supports 28V high voltage input pin (PTA3) for wakeup
  - 1 GPIO connects to LIN pad
- Two kinds of 32 QFN packages
  - Single end mode
  - Differential mode
- Operating characteristics
  - Normal operating voltage: 5.5V ~ 28V (operating voltage up to 36V limited to 24h over lifetime) with full functional flash program/erase/read operations
  - Ambient operation temperature: -40°C ~ 150°C
  - Junction operation temperature: -40°C ~ 175°C

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2 Overview

YTM32Z1MC0x series provide a highly scalable portfolio of ARM® Cortex®-M0+ MCUs in the automotive industry. This series integrates high-voltage modules, including the voltage regulator(LDO), Pre-driver and Local Interconnect Network(LIN) physical layer. These features enable a fully integrated single-chip solution to drive up to 8 external power MOSFETs for BLDC or PMSM motor drive applications. With a 5.5v~28V power supply and rich peripherals such as PREDRV, ADC, ZDU, TEMPSENSOR, SPI, UART, LIN-PHY, GPIO and protection functions such as overcurrent protection, overvoltage protection, undervoltage protection and overtemperature protection. It is very suitable for application such as small BLDC water pumps, oil pumps, DC motor drivers for window lifts and so on.

3 Block Diagram

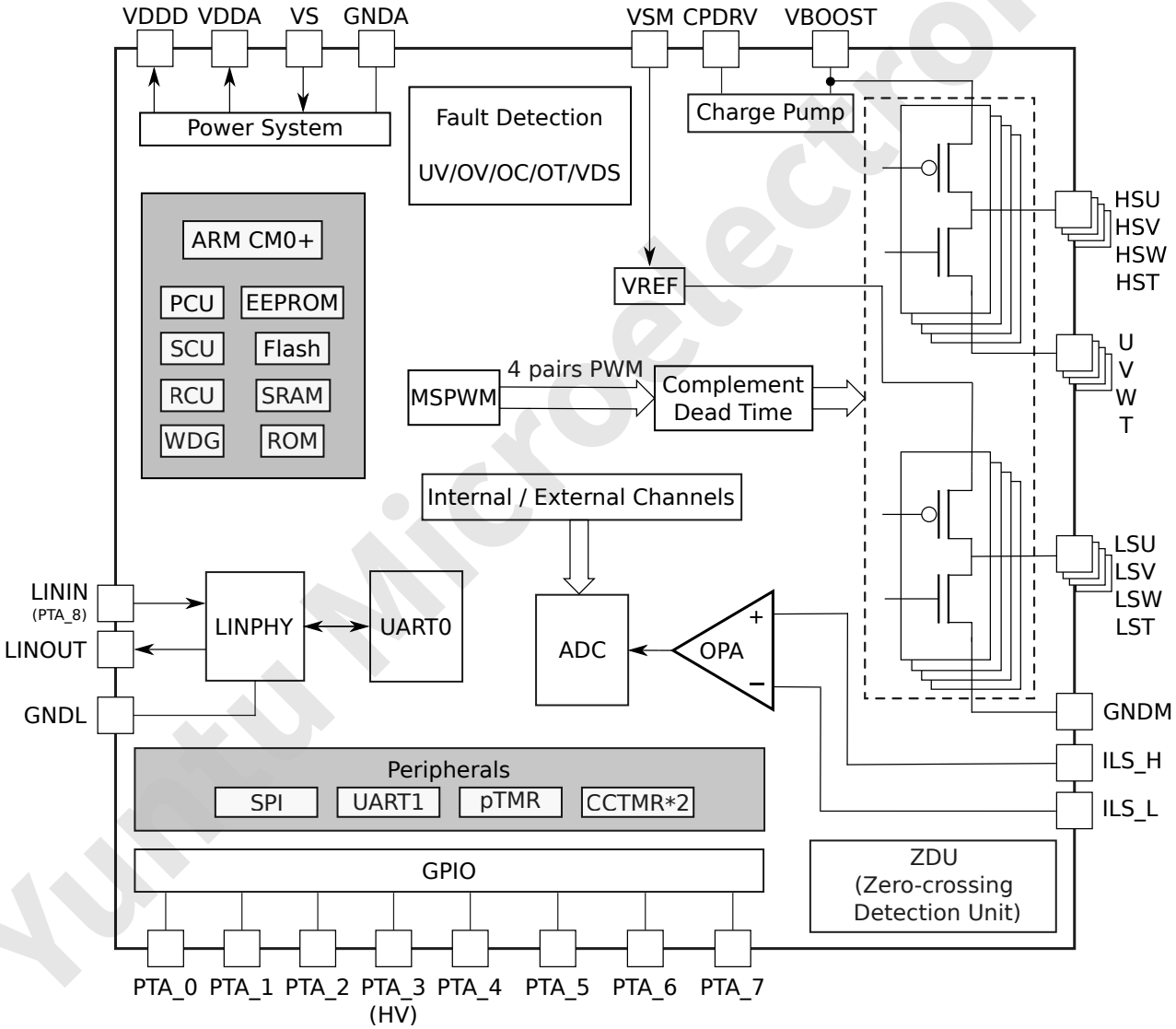


Figure 1: YTM32Z1MC0x Block Diagram

4 Features

The following sections describe the high-level module features for YTM32Z1MC0x device.

4.1 Core and System Modules

4.1.1 ARM Cortex-M0+

- Up to 48 MHz core frequency
- Supports up to 32 interrupt request sources
- 2 stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Single cycle 32 bits by 32 bits multiplier

4.1.2 Nested Vector Interrupt Controller (NVIC)

- Up to 16 internal interrupt sources and 32 external interrupt sources
- Supports four priority levels for interrupts with two bits in each IPRn registers

4.1.3 Debug Controller

- 2-pin Serial Wire Debug (SWD) provides external debugger interface

4.1.4 System Clock Unit (SCU)

- Provide fixed system clock divider to generate bus clock(1/2 frequency of core clock)
- Provide glitch free switcher to select system clock source from OSC and PLL
- Internal RC Oscillator(OSC)
  - 2MHz
  - Default system boot clock source
  - PLL reference clock
  - Support working in deepsleep mode
  - Support trim for temperature and process
- Phase-locked Loop(PLL)
  - Up to 48MHz
  - Can be selected as system clock source
  - Support working in deepsleep mode(with OSC working in deepsleep mode)
  - Contain PLL frequency lock detector, support configurable reset when PLL lock is lost
- Low Power Oscillator (LPO)
  - 10KHz
  - Can be selected as function clock source
  - Support working in all low power modes including Powerdown mode

4.1.5 Power Control Unit (PCU)

- Combination of internal and external voltage regulator options, offering run and Powerdown mode
- Active POR providing brown-out detect
- Low Voltage Reset (LVR) for all system relevant power domains
- VS Low Voltage Detect (VSLVD, with configurable debounce) as indication for software
- VSM Over Voltage Monitor(VSMOVM, with configurable debounce) indication for software
- Over Temperature Detect(OVT, with configurable debounce) indication for software

- Over Current Driving Detect(OCDRV, with configurable debounce) indication for software
- Wake up sources(LIN, PTA3 and LPWDT) in Powerdown mode indication for software
- Support trim for reference current, bandgap and LDO

4.1.6 Reset Controller Unit (RCU)

- Record the reset sources of most recent resets
- Configurable filter for reset pin
- Reset pin filter can work in RUN, Sleep and Deepsleep mode

4.1.7 IP Controller (IPC)

- Peripheral Bus clock enable
- IPC clock source selection as follow
  - Bus clock
  - OSC clock
  - LPO clock
- Peripheral software reset

4.1.8 Divide and Square Root (DIVSQRT)

- Lightweight implementation of 32-bit integer divide and square root arithmetic operations
  - Supports 32/32 signed and unsigned divide (or remainder) calculation
  - Supports 32-bit unsigned square root calculation
- Simple programming model includes registers of input data, result, control, status
- Programming model interface optimized for activation from inline code or software library call
  - “Fast Start” configuration minimizes the memory-mapped register write overhead
  - Supports two methods to determine when the result is valid, including software polling
  - Configurable divide-by-zero response
- Pipelined design process 2bits per cycle with early termination exit for minimum execution time

4.1.9 Trigger Multiplex Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources

4.1.10 Chip Integration Module (CIM)

- System function configuration
- LIN PAD function selection
- Software trigger generation
- Chip and die information

4.1.11 On-chip Memories

4.1.11.1 Embedded Flash Module (EFM)

- 32K Bytes PFlash with ECC
- 192 Bytes EEPROM
- 2KB sector size and 128 Bytes program page size for PFlash
- Automated program and erase operation for PFlash

- Automated recall and store operation for EEPROM
- Optional interrupt on command completion
- Security for single-chip applications

4.1.11.2 Static Random Access Memory (SRAM)

- 4K Bytes SRAM with ECC

4.1.11.3 Read Only Memory (ROM)

- 16K Bytes ROM
- Support LIN boot loader function which follows simple UDS protocol
- Support NAD configurable
- Support polling window width configurable
- Support WDG function configurable to work or not
- Integrate common motor FOC control function
  - Clark Park function
  - Circle limit function
  - Single resister sample phase current calculation
  - PWM phase change for single resister sample and sample point calculation
  - STO-PLL observer function
  - SVPWM calculation function

4.2 Communication Interfaces

4.2.1 Universal Asynchronous Receiver/Transmitter (UART)

- Support LIN 1.3, 2.0, 2.1, 2.2A and SAE J2602
- Support LIN break send and detect
- Baudrate setting
- 1-bit or 2-bit STOP size
- 7-bit, 8-bit, 9-bit or 10-bit frame size
- Transmit/Receive polarity setting
- Receive data match
- Line idle, address match wakeup
- Support transmit/receive line switch

4.2.2 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration
- Configurable frame size
- Support single line mode
- Support master and slave mode

4.2.3 Local Interconnect Network Physical Layer (LINPHY)

- Support LIN 2.x standard
- LIN slave controller and transceiver
- Baud rate up to 20 Kbps

- Support waking up system by LIN frame
- Support reusing LINPHY pin with CCTMR, GPIO and UART0

4.3 Timer

4.3.1 Periodic Timer (pTMR)

- Timers can generate interrupts and each channel can generate independent interrupt request
- Four channels of 16-bit timers, each timer has independent timeout periods
- Ability to stop in debug mode
- Support chain mode to connect multiple timers to a longer timer

4.3.2 Motor Specific Pulse Width Modulation (MSPWM)

- Contain a 16-bit counter
  - Configurable final counter value
- Support 7-bit clock prescaler
- PWM mode
  - Complementary mode
  - Independent mode
- Support double buffers and registers loading mechanism
- Support double switch logic
- Support generating triggers
  - Output triggers on match point
  - Output window by PWM or related combination logic
- Support GTB (Global Time Base)
- Support several interrupts
  - Channel interrupt
  - Counter overflow interrupt
- Support counter running under debug mode

4.3.3 Capture and Compare Timer (CCTMR)

- Contain a 16-bit counter
  - Configurable final counter value
- Counter counting mode
  - One shot mode
  - Free run mode
- Support 7-bit clock prescaler
- Support three channel modes
  - PWM mode
    - Independent mode for each channel
  - Output Compare mode
    - The output can be configured to set, clear or toggle on match point
  - Input Capture mode
    - Support rising edges, falling edges or dual edges capture
    - Support input filter with a prescaler
    - Support capture test mode
- Support generating triggers
  - Output triggers on match point

  - Output pulse with adjustable width by PWM
- Support GTB (Global Time Base)
- Support several interrupts
  - Channel interrupt (capture/compare interrupts)
  - Counter overflow interrupt
- Support counter running under debug mode

4.4 Analog

4.4.1 Analog-to-Digital Converter (ADC)

- Support 10-bit single-end fixed resolution
- Up to 1Msps for 10-bit resolution conversion performance
- Support up to 24 input channels
  - 8 channels to measure external analog signals from pad
  - 16 channels to measure internal signals
- Support multiple conversion modes
  - Single mode
  - Continuous mode
  - Discontinuous mode
- Support sequence length switch by trigger when the previous sequence conversion is completed
- Support software/hardware trigger for ADC start conversion
- Support two low power modes
  - Wait mode: prevent ADC overrun when FIFO is full
  - Auto off mode: automatic control ADC power off
- Support watchdog for conversion result monitoring
- Support interrupt generation
  - Ready for conversion
  - End of sampling
  - End of conversion
  - End of sequence conversion
  - Overrun event
  - Watchdog event
  - Error event
- Selectable reference voltage 0.75V, 1.5V and 2.5V

4.4.2 Pre-Driver (PREDRV)

- Drive U/V/W/T four phases
- Integrate PWM mutex circuit
- Dead time insert
  - Internal pre-driver dead time insert
  - External FET dead time insert
- Fault monitor and safety mechanism
  - Internal fault monitor
    * Under voltage fault
    * Over voltage fault
    * Over current fault
    * Over temperature fault
    * VDS fault

  - Customized fault monitor
- Register access protection
- Interrupt

4.4.3 Zero-crossing Detection Unit (ZDU)

- Integrate a comparator internally
- Functional mode
  - Common mode
  - Window mode
- Integrate a virtualize central point internally
- Observation of internal signals by PIN
- Comparator output filter
- Comparator output trigger
- Generate interrupt on rising-edge, falling-edge or both edges of the comparator output

4.5 Safety

4.5.1 Watchdog (WDG)

- 16-bit countdown timer
- Support regular or window servicing mode
- Support reset request or interrupt for first timeout
- Support fixed key for dog feeding
- Hard and soft configuration lock bits

4.6 Human Machine Interface

4.6.1 General Purpose Input/Output (GPIO)

- Port Data Input register
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Output enable register
- Digital filter for data inputs, but all GPIOs share the filter width configuration
- Inversion for data inputs
- Interrupt flag and enable registers for each pin
- Support for edge sensitive (rising, falling, both) or level sensitive (low, high)
- Asynchronous wake-up in low-power modes
- Pin interrupt is functional for all pins

4.6.2 Port Controller (PCTRL)

- Individual pull control fields with pull-up, pull-down, and pull-disable support
- Individual mux control field supporting analog or pin disabled, GPIO, and up to 7 chip-specific digital functions
- Individual open drain control support

5 Ordering Information

The following chips are available for ordering.

Table 1: Ordering Table

Product	Memory				Package		IO Channel		
Part Number	Flash	EEPROM	SRAM	ROM	Pin Count	Package	Normal IO	High Voltage IO	LIN IO
YTM32Z1MC03X0WFMST	32KB	192B	4KB	16KB	32	QFN	7	1	1
YTM32Z1MC03X0WFMDT	32KB	192B	4KB	16KB	32	QFN	7	1	1

5.1 Part Number Information

YTM32Z1MC0x part numbers field is shown as below.

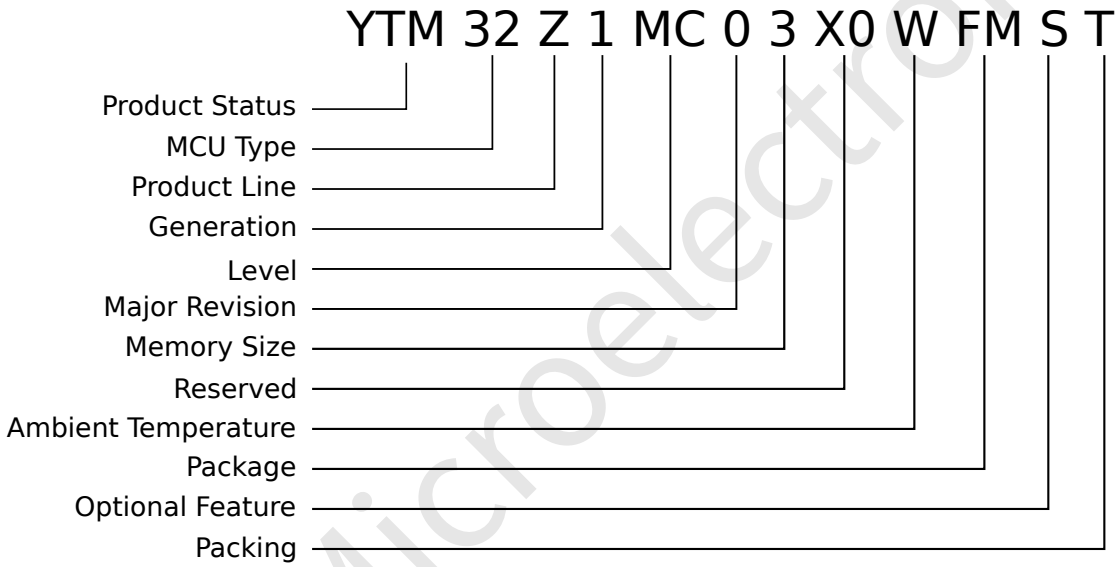


Figure 2: YTM32Z1MC0x Part Numbers Field

The part numbers field description is shown as below.

Table 2: Part Number Field Description

Field	Description	Values
YTM	Product Status	YTM: Qualified PTM: Prototype
32	MCU Type	32: 32-bit
Z	Product Line	Z: High voltage, integrity
1	Generation	1st generation production
Mx	Level	M: Motor+LIN-PHY L: LIN-PHY C: CAN-PHY T: Touch-sensor
0	Major Revision	1st revision

Field	Description	Values				
3	Memory Size	1	2	3	4	5
		8K	16K	32K	64K	128K
X0	Reserved	Reserved				
W	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C				
FM	Package	Pins	LQFP	QFN	BGA	-
		32	LE	FM	-	-
		48	LF	-	-	-
		64	LH	-	-	-
		100	LL	-	MH	-
		144	LQ	-	-	-
		176	LU	-	-	-
		257	-	-	MM	-
		289	-	-	MQ	-
S	Optional Feature	S: Single end mode D: Differential mode				
T[1]	Packing	T: Trays/Tubes R: Tape and Reel				

1. The chip mark doesn't contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ W-Grade\ Part}$	Ambient temperature under bias	-40	–	150	°C
$T_{J\ W-Grade\ Part}$	Junction temperature under bias	-40	–	175	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model, except LIN pin	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	-500	500	V	
	Corner pins only	-500	500	V	
I_{LAT}	Latch-up current at ambient temperature of 150 °C at any pin	-100	100	mA	3
	Latch-up current at ambient temperature of 25 °C at any pin	-200	200	mA	
I_{LAT_DRIVE}	Latch-up current at ambient temperature of 150 °C at drive pin	-250	250	mA	4
	Latch-up current at ambient temperature of 25 °C at drive pin	-250	250	mA	
V_{HBM_LIN}	Electrostatic discharge voltage, human body model, only LIN pin	-6000	6000	V	5
V_{IEC_LIN}	Electrostatic discharge voltage, human body model, only LIN pin	-6000	6000	V	6

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).
Equivalent to discharging a 100pF capacitor through a 1.5kΩ resistor.
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for
Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.
4. @t=10 sec.
5. Determined according to AEC-Q100-002, ESD is applied on LIN pin against shorted GND pins.
Equivalent to discharging a 100pF capacitor through a 1.5kΩ resistor.
6. Equivalent to discharging a 150pF capacitor through a 330Ω resistor conform to IEC standard 1000-4-2.

6.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Limit Min	Max	Unit
Battery supply voltage	V_S		-0.5	28(36V[4])	V
		t < 500 ms	-0.5	45	V
	V_{SM}		V_{DDA}-0.3	28 (36V[4])	V
		t < 500 ms	V_{DDA}-0.3	45	V
	$V_{S.tr1}$	ISO 7637-2 pulse 1[1] V_S=13.5V, T_A=(23 ± 5)°C	-100		V
	$V_{S.tr2}$	ISO 7637-2 pulse 2[1] V_S=13.5V, T_A=(23 ± 5)°C		75	V
	$V_{S.tr3}$	ISO 7637-2 pulse 3A, 3B[1] V_S=13.5V, T_A=(23 ± 5)°C	-150	100	V
Battery supply current	I_{VSM_max}	maximum DC or RMS supply current VSM		125	mA
Output voltage	V_{DDA}		-0.3	3.6	
Output voltage	V_{DDD}		-0.3	1.95	

Table 6 continued from previous page

Parameter	Symbol	Condition	Limit Min	Max	Unit
LIN Bus	V_{LIN}	T < 500ms	-27	45	V
	$V_{BUS.tr1}$	ISO 7637-2 pulse 1[2] V_S=13.5V, T_A=(23 ± 5)°C	-100		V
	$V_{BUS.tr2}$	ISO 7637-2 pulse 2[2] V_S=13.5V, T_A=(23 ± 5)°C		75	V
	$V_{BUS.tr2}$	ISO 7637-2 pulse 3A, 3B[2] V_S=13.5V, T_A=(23 ± 5)°C	-150	100	V
	I_{LIN_max}	Maximum current in LININ or LINOUT	-200	200	mA
Voltage on Analogue HV	V_{ANA_HV}	PTA3 with internal divider T, U, V, W outputs[3]	-0.3	V_S+0.3	V
Voltage on PIN VBOOST	V_{AN_VBOOST}	switching transients at 36V motor drive		45	V
Voltage on Analogue HV	V_{AN_HSx}		-0.3	V_{BOOST}+0.3	V
Voltage on Analogue HV	V_{AN_LSx}		-0.3	V_{REF}+0.3	V
Voltage on pin ILS	V_{ILS_H}, V_{ILS_L}		-0.5	V_{DDA}+0.3	V
Voltage on PTA[7:4] and PTA[2:0]	V_{PTA_LV}		-0.3	V_{DDA}+0.3	V
Voltage on PTA[3]	V_{PTA_HV}		-0.3	V_S+0.3	V
Current on PTA[7:0]	I_{IN_IO}		-10	10	mA

1. ISO 7637 test pulses are applied to V_S via a reverse polarity diode and >22μF/100nF blocking capacitor; ISO 7637 test pulses for 24V car battery needs to be protected by external components.
2. ISO 7637 test pulses are applied to BUS via a coupling capacitance of 1nF; ISO 7637 test pulses for 24V car battery needs to be protected by external components.
3. In case of negative voltages applied on T, U, V, W pins, voltage can go lower than -0.3V.
4. 36V operation is limited to maximum 24 hours over life; 28..36V motor driving may require 100..500 Ohm resistor at VBOOST pin to protect in case of PCB switching transients >45V.

6.3 Peripheral Parameters

6.3.1 Clock Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Frequency of the Internal RC oscillator	F_{rc_osc}	RC oscillator is trimmed	1.97	2	2.03	MHz
Frequency of the PLL	F_{PLL}	RC oscillator is trimmed, and PLL is configured as 40MHz@150°C	39.4	40	40.6	MHz
		RC oscillator is trimmed, and PLL is configured as 48MHz@105°C	47.28	48	48.72	MHz

Table 7 continued from previous page

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Settling time of the PLL	T_{setPLL}	RC oscillator is trimmed, and PLL is switched on		2		ms
Frequency of the low power oscillator	F_{lpo_clk}		5	10	20	KHz
Startup time of the system after power on	T_{por}	C_{VDDA}=C_{VDDD}=100nF; time until the first Flash instruction can be executed.			TBD	ms
Startup time of the Charge pump	T_{pump}	Time from Charge pump start till V_{BOOST}=V_S+6V for V_S>12V; motor not running during startup, C_{fly}=100nF, C_{BOOST}=1μF			5	ms

6.3.2 Regulator Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
3.3V regulator	V_{DDA}	After trimmed	3.15	3.3	3.45	V
Output current capability	I_{DDout_vdda}				25	mA
1.8V regulator	V_{DDD}	After trimmed	1.77	1.85	1.93	V
Output current capability	I_{DDout_vddd}				0	mA

6.3.3 Power Mode Transition Operating Behaviors

Description	System clock	Frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	OSC	2MHz	–	970ns	–
DEEPSLEEP -> ACTIVE	OSC	2MHz	–	2.12ms	–
POWERDOWN -> ACTIVE	OSC	2MHz	–	448μs	–
T_{POR}	OSC	2MHz	–	560μs	–

6.3.4 Power Consumption

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max	Unit
ACTIVE	I_{DD_ACTIVE}	PLL	Running coremark in flash, all peripheral clock enabled. core @48MHz, bus @24MHz V_S=12V	25 °C	–	11.6	–	mA
				150 °C	–	12.3	–	mA

Table 10 continued from previous page

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max	Unit
			Running coremark in flash, all peripheral clock disabled. core @48MHz, bus @24MHz V_S=12V	25 °C	–	9.3	–	mA
				150 °C	–	10.0	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @48MHz, bus @24MHz V_S=12V	25 °C	–	10.9	–	mA
				150 °C	–	11.6	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @48MHz, bus @24MHz V_S=12V	25 °C	–	8.6	–	mA
				150 °C	–	9.3	–	mA
		OSC	Running coremark in flash, all peripheral clock enabled. core @2MHz, bus @1MHz V_S=12V	25 °C	–	2.1	–	mA
				150 °C	–	2.7	–	mA
			Running coremark in flash, all peripheral clock disabled. core @2MHz, bus @1MHz V_S=12V	25 °C	–	2.0	–	mA
				150 °C	–	2.6	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @2MHz, bus @1MHz V_S=12V	25 °C	–	2.1	–	mA
				150 °C	–	2.7	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @2MHz, bus @1MHz V_S=12V	25 °C	–	2.0	–	mA
				150 °C	–	2.6	–	mA
SLEEP	I_{DD_SLEEP}	PLL	Sleep mode current, core @2MHz, bus @1MHz V_S=12V	≤ 25 °C	–	5.2	–	mA
				150 °C	–	5.7	–	mA
DEEPSLEEP	$I_{DD\_DEEPSLEEP}$	PLL	Deepsleep mode current, V_S=12V OSC, PLL enable	≤ 25 °C	–	1.3	–	mA
				150 °C	–	1.8	–	mA
			Deepsleep mode current, V_S=12V OSC enable, PLL disable	≤ 25 °C	–	526.0	–	μA
				150 °C	–	985.3	–	μA
			Deepsleep mode current, V_S=12V OSC, PLL disable	≤ 25 °C	–	419.0	–	μA
				150 °C	–	865.1	–	μA
POWERDOWN	$I_{DD\_POWERDOWN}$	PLL	Powerdown mode current, V_S=12V	≤ 25 °C	–	26.1	–	μA
				150 °C	–	58.1	–	μA

6.3.5 IO Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Leakage current in PTA[7:0]	I_{leakio}	1/16 divider on PTA3 disabled	-5		5	μA
Digital high input threshold level	V_{ih}		2.4			V
Digital low input threshold level	V_{il}				1	V
Digital input hysteresis	$V_{inhystio}$		0.1			V
PTA3 wakeup threshold level	V_{wu_lh}	Active in Powerdown mode	2.7			V
PTA3 wakeup threshold level	V_{wu_hl}	Active in Powerdown mode			1.2	V
PTA3 wakeup hysteresis	V_{hystio_wu}	Active in Powerdown mode	0.1			V
Output voltage low	V_{outl_pta}	PTA[7:4,2:0], I_{load}=2mA			0.4	V
Output voltage high	V_{outh_pta}	PTA[7:4,2:0], I_{load}=2mA	VDDA - 0.4			V
Output voltage low	V_{outl_pta3}	PTA3, I_{load}=1mA			0.4	V
Output voltage high	V_{outh_pta3}	PTA3, I_{load}=1mA	VDDA - 0.4			V
Input voltage range for ADC	$V_{in\_adc\_pta[7:4,2:0]}$	For information only	0		2.5	V
Input voltage range for ADC	$V_{in\_adc\_pta3}$	For information only	0		36	V

6.3.6 ADC Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
ADC full scale range	F_{sr3}	ADC_REF=2'b11	2.45	2.5	2.55	V
	F_{sr2}	ADC_REF=2'b10	1.47	1.5	1.53	V
	F_{sr1}	ADC_REF=2'b01	0.735	0.75	0.765	V
	F_{sr0}	ADC_REF=2'b00		off		V
Differential nonlinearity	DNL	Only characterized; no production tset	-1		1	LSB
Integral nonlinearity	INL	Only characterized; no production tset	-3		3	LSB
Minimum conversion time	T_{conv}	adc_clk=48MHz	0.625			μs
Minimum sampling time	T_{samp}	Time between channel select and start of conversion	0.375			μs
Channel set up time	T_{setup}	With channel change	3			μs
Minimum time between 2 ADC conversions	T_{cycl}	adc_clk=48MHz; without channel change	1			μs
		with channel change	4			μs
ADC error(excluding ADC reference and INL)	Err_{ADC}	LV channels	-1		1	%
		HV channels(with predivider)	-3		3	%

6.3.7 Voltage Detect Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
POR off	V_{por_lh}	Only for information		3.6		V
POR on	V_{por_hl}	Only for information		3.15		V
Hysteresis for POR	V_{hyst_por}	Only for information	60			mV
VS Programmable range for undervoltage level	V_{uv_range}	LVDT_VS_CFG[2:0]=000	3.5	4	4.5	V
		LVDT_VS_CFG[2:0]=001	4.5	5	5.5	V
		LVDT_VS_CFG[2:0]=010	5.5	6	6.5	V
		LVDT_VS_CFG[2:0]=011	6.5	7	7.5	V
		LVDT_VS_CFG[2:0]=100	7.5	8	8.5	V
		LVDT_VS_CFG[2:0]=101	8.5	9	9.5	V
Hysteresis for VS undervoltage detect	V_{hyst_uv}		0.1		1	V
Debouncing for VS undervoltage detect	T_{uv}	Only for information	10	30	60	μs
VDDA undervoltage reset on	$V_{uvr\_hl\_VDDA}$		2.7	2.85	3	V
VDDA undervoltage reset off	$V_{uvr\_lh\_VDDA}$		2.85	3	3.15	V
Hysteresis for undervoltage reset	$V_{hyst\_uvr\_VDDA}$	Guaranteed by design	0.1			V
Debouncing for VDDA undervoltage reset	T_{uvr_VDDA}		1	3	10	μs
VDDD undervoltage reset on	$V_{uvr\_hl\_VDDD}$		1.525	1.6	1.675	V
VDDD undervoltage reset off	$V_{uvr\_lh\_VDDD}$		1.6	1.675	1.75	V
Hysteresis for undervoltage reset	$V_{hyst\_uvr\_VDDD}$	Guaranteed by design	0.05			V
Debouncing for VDDD undervoltage reset	T_{uvr_VDDD}		1	3	10	μs
Level for load dump interrupt on	V_{ld_lh}	VSM_OV_VSEL=0	31.5	33	34.5	V
		VSM_OV_VSEL=1	37	38.5	40	V
Level for load dump interrupt off	V_{ld_hl}	VSM_OV_VSEL=0	29.5	31	32.5	V
		VSM_OV_VSEL=1	34.5	36	37.5	V
Hysteresis for load dump interrupt	V_{hyst_ld}		1	2	3	V
Debouncing for load dump interrupt	T_{ld}	Only for information	50		100	μs

6.3.8 Tempsensor Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Over temperature shutdown interrupt	T_{ot_on}	Tested by special test mode	170	180	190	°C
	T_{ot_off}		140	150	160	°C
	T_{ot_hyst}	Guaranteed by design	10			°C
Temperature range	T_{range}	Sensor measures IC junction temperature	-40		180	°C

Table 14 continued from previous page

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Temperature measurement gain	T_{temp_gain}			0.5		°C/LSB
Accuracy	T_{acc}	Guaranteed by design, after calibration	-10		10	°C

6.3.9 VSM Sensor Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input range	VSM_min		5.5			V
	VSM_max	ADC_REF=2'b11			36	V
		ADC_REF=2'b10			24	V
		ADC_REF=2'b01			12	V
Output capability	$T_{settling\_ADC}$	Time to charge the ADC sampling capability, only information, no production test		0.3	0.5	μs
Low-pass filter cut-off frequency	F_{vsm_filter}	-3dB cutoff frequency, only information	0.7		3.5	kHz
VSM sensor filter offset	$V_{adc\_vsm\_offset}$	Referred to input voltage of VSM	-400		400	mV

6.3.10 PREDRV Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Low side FET gatedrive voltage	V_{REF_LS}	$V_{SM} \geq 7V$	6	8	9	V
		$5V<V_{SM}<7V$	V_{SM}-1			V
Low side Ron charge	R_{LS_HIGH}	$V_S=V_{SM}=8\sim36V$, test at 13V in production	10	30	65	Ω
Low side Ron discharge	R_{LS_LOW}	$V_S=V_{SM}=8\sim36V$, test at 13V in production	10	25	55	Ω
High side Ron charge	R_{HS_HIGH}	$V_S=V_{SM}=8\sim36V$, test at 13V in production	8	40	80	Ω
High side Ron discharge	R_{HS_LOW}	$V_S=V_{SM}=8\sim36V$, test at 13V in production	8	40	90	Ω
Chargepump output voltage	V_{BOOST}	$V_{SM} \geq 10V$	V_{SM}+7	V_{SM}+8	V_{SM}+9.5	V
		$8V \leq V_{SM}<10V$	V_{SM}+5.5		V_{SM}+9.5	V
		$5.5V<V_{SM}<8V$	V_{SM}+3		V_{SM}+8	V

Table 16 continued from previous page

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
CPDRV output resistance	R_{CPDRV_HIGH}	I_{load}=2mA, test at 13V in production	15	40	120	Ω
	R_{CPDRV_LOW}	I_{load}=2mA, test at 13V in production	10	26	60	Ω
	F_{CP_FREQ}		40	50	60	kHz
Dead time	T_{DEAD}	Programmable with 8 bits.	0	1.0	5.3	μs
Predrv current sensor input range	V_{CURR_IR}	Allowed input range of shunt voltage, for information only	-100		100	mV
Current sensor gain	A_{cs}		9.5	10	10.5	
Current sensor reference	V_{cs0}	V_{ILS}=0(the value of common-mode voltage)		1.25		V
Current sensor calibration error	V_{cs_err}	Measured at the output of the current sensor	-20		20	mV
Current sensor low	T_{cs_filter}	Guaranteed by design	0.25	0.5	1	μs
Overcurrent detection	V_{oc}		260	300	330	mV
Debouncing for overcurrent (Programmable with 2 bits)	T_{oc}	PCU_OCCR[OC_DEB_CFG]=00	1	1.5	2	μs
		PCU_OCCR[OC_DEB_CFG]=01	2	3	4	μs
		PCU_OCCR[OC_DEB_CFG]=10	4	6	8	μs
		PCU_OCCR[OC_DEB_CFG]=11	8	12	16	μs
External FET detection level	V_{ds}	V_{ds} over voltage level when FET is on	1.5	2	2.5	V
Filter Time	T_{vds}	Time from FET on till V_{ds} monitoring start. Programmable with 8 bits.	0	1.6	5.3	μs
Input common voltage of zero-detect comparator	V_{cm_zdc}		-0.1		1.5	V
Input error of zero-detect comparator	V_{zdc_err}		1		20	mV
Delay of zero-detect comparator	T_{zdc_dly}				1.4	μs

6.3.11 LIN Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Short circuit bus current	I_{BUS_LIM}	V_{BUS}=V_{BAT}=18V, driver on	40		200	mA
Pull up resistance bus, normal and standby mode	R_{SLAVE}		20		60	kΩ
Pull up current, sleep mode	$I_{LIN\_PU\_SLEEP}$	V_{BUS}=0V, V_{BAT}=12V, sleep mode	-100			μA
Input leakage at the receiver incl.PU	$I_{BUS\_PAS\_dom}$	V_{BUS}=0V, V_{BAT}=12V	-1			mA
		V_{BUS}=0V, $V_{BAT=24V}$	-2			mA
Bus reverse current, recessive	$I_{BUS\_PAS\_rec}$	Driver off, 8V<V_{BAT} ≤ 27V			20	μA
		27V< V_{BAT}<36V			50	μA
Bus reverse current, loss of battery	$I_{BUS\_NO\_BAT}$	V_S=0V, 0V<V_{BUS}<18V		1	23	μA
		18V< V_{BUS}<36V			100	μA
Bus current during loss of ground	$I_{BUS\_NO\_GND}$	V_S=V_{GND}=12V, V_{BUS}=0V ~ 18V	-1		1	mA
		V_S=V_{GND}=24V, V_{BUS}=0V ~ 36V	-2		2	mA
Transmitter dominant voltage	V_{olbus}	Network load=500Ω, TxD=0	0		0.2	VS
Transmitter recessive voltage	V_{ohbus}	TxD open	0.8		1	VS
BUS input capacitance	C_{BUS}	Only information		25	35	pF
Receiver dominant voltage	V_{BUSdom}				0.4	VS
Receiver recessive voltage	V_{BUSrec}		0.6			VS
Centre point of receiver threshold	V_{BUS_CNT}	V_{BUS_CNT}=(V_{BUSdom}+V_{BUSrec})/2	0.475	0.5	0.525	VS
Receiver hysteresis	V_{BUS_hys}	V_{BUS_hys}=V_{BUSres}-V_{BUSdom}	0.15		0.175	VS
Propagation delay receiver[125]	T_{rx_pdf}	$C_{RxD=25pF}$ Falling edge			6	us
Propagation delay receiver[125]	T_{rx_pdr}	$C_{RxD=25pF}$ Rising edge			6	us
Propagation delay receiver symmetry[5]	T_{rx_sym}	T_{rx_pdf} - T_{rx_pdr}	-2		2	us
Receiver debounce time[6]	T_{rec_deb}	LIN rising and falling edge	0.5		4	us
LIN duty cycle 1[23]	D1	20kbps operation, normal mode	0.396			
LIN duty cycle 2[23]	D2	20kbps operation, normal mode			0.581	
LIN duty cycle 3[23]	D3	10.4kbps operation, low speed mode	0.417			
LIN duty cycle 4[23]	D4	10.4kbps operation, low speed mode			0.59	
$T_{rec(max)}$ - $T_{dom(min)}$ [4]	Δt3	10.4kbps operation, low speed mode			15.9	μs
$T_{rec(min)}$ - $T_{dom(max)}$ [4]	Δt4	10.4kbps operation, low speed mode			17.28	μs
TxD dominant timeout	t_{TxD_to}	Normal mode, $V_{TxD=0V}$		64		ms

1. This parameter is tested by applying a square wave signal to the LIN. The access to internal signals RxD, TxD will be performed by test mode. The minimum slew rete for the LIN rising and falling edge is 50V/μs.
2. See Figure3:LIN timing diagram
3. Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal termination disabled
4. In accordance to SAE J2602
5. Parameter in relation to internal signal TxD
6. Internal value to suppress spikes; only proved during characterization:not measured in production

As shown in figure, both worst case duty cycles can be calculated as follows:

$$D_{wc1} = t_{BUS\_Rec(min)}/2 * t_{Bit}$$
$$D_{wc2} = t_{BUS\_Rec(max)}/2 * t_{Bit}$$

Thresholds for duty cycle calculation in accordance to LIN2.x:

Baud rate	20kBaud	10.4kBaud
t_{Bit}	50μs	96μs
D_{wc1}	D1	D3
D_{wc2}	D2	D4
$TH_{REC(MAX)}$	0.774 V_{S_TX}	0.778 V_{S_TX}
$TH_{DOM(MAX)}$	0.581 V_{S_TX}	0.616 V_{S_TX}
$TH_{REC(MIN)}$	0.422 V_{S_TX}	0.389 V_{S_TX}
$TH_{DOM(MIN)}$	0.284 V_{S_TX}	0.251 V_{S_TX}

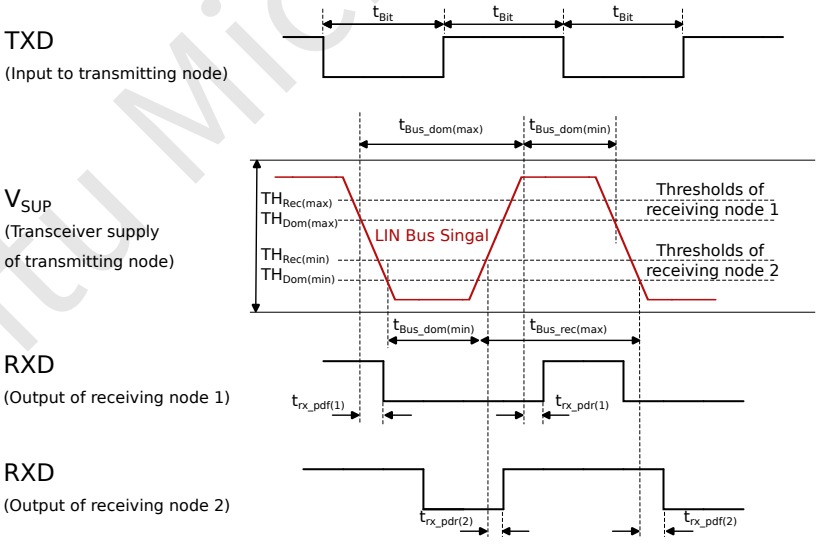


Figure 3: LIN Timing Diagram

6.3.12 NVM Flash Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Write time	T_{write}		5		6	ms
Erase time	T_{erase}		20		21	ms
Read access time	T_{acc}	Tj=-40°C ~ 125°C		49.5		ns
		Tj=-40°C ~ 175°C		55.4		ns
Read temperature	T_{read_fls}		-40		175	°C
Program and erase temperature	T_{pg_fls}		-40		125	°C
Cycling endurance	$T_{nvmcycp}$	Tj@125°C	1000			cycle
Data retention	T_{nvmret}	Tj ≤ 85°C	20			years
		Tj ≤ 125°C	10			years
		Tj ≤ 150°C	3			years
		Tj ≤ 175°C	1			years

6.3.13 EEPROM Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Cycling endurance	$T_{nvmcycp}$	Tj@25°C	100000			cycles
		Tj@125°C	10000			cycles
		Tj@150°C	10000			cycles
		Tj@175°C	1000			cycles
Data retention	T_{nvmret}	Tj@125°C	10			years
		Tj@150°C	3			years
		Tj@175°C	1			years

6.3.14 Debug Module Electrical

6.3.14.1 SWD Electrical Specifications

Table 21: SWD Full Voltage Range Electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns

Table 21 continued from previous page

Symbol	Description	Min.	Typ.	Max.	Unit
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

6.3.14.2 SWD Input Clock Timing

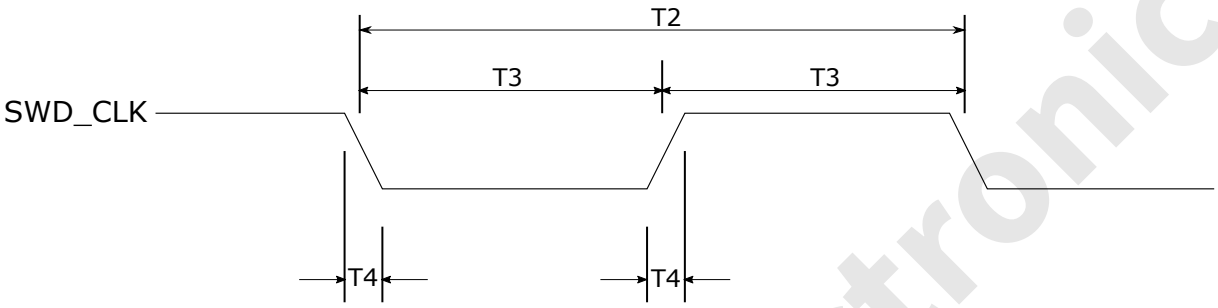


Figure 4: SWD Clock Timing

6.3.14.3 SWD Output Data Timing

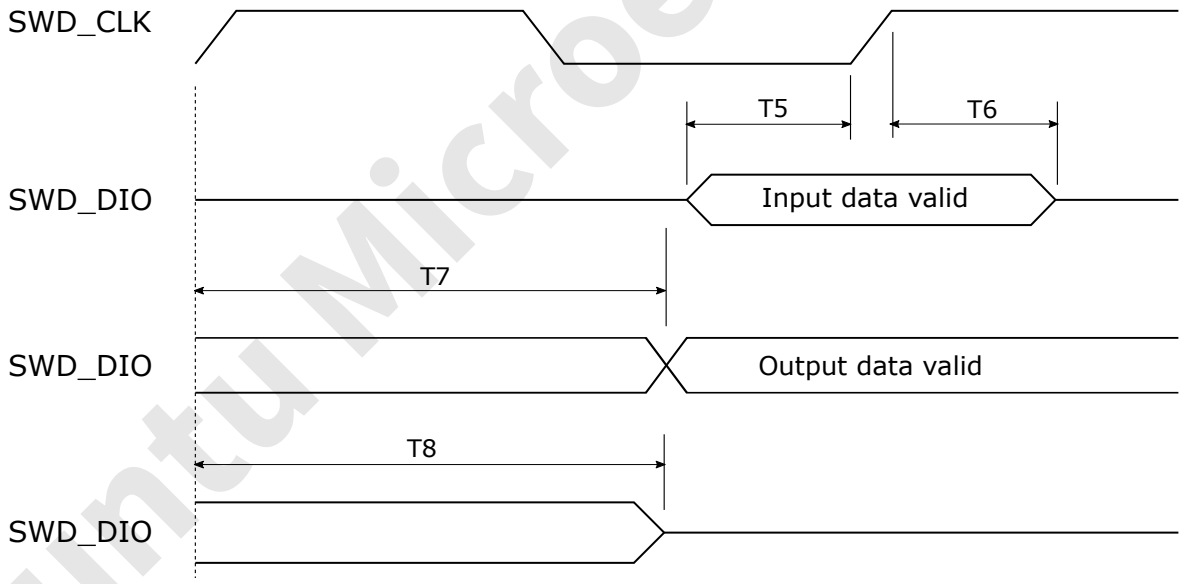


Figure 5: SWD Data Timing

6.4 Thermal Attributes

Table 22: Thermal Characteristics

Package Family	Package Type	Thermal Resistance JA (°C/W)
QFN	QFN32L	41

7 Pinouts

7.1 IO Signal Description

YTM32Z1MC0x supports two kinds of QFN package, including 32 QFN single end mode and differential mode as follows:

Table 23: Pinmux Table

32QFN Single End	32QFN Differential	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	W	W	-	-	-	-	-	-	-
2	2	HSV	HSV	-	-	-	-	-	-	-
3	3	V	V	-	-	-	-	-	-	-
4	4	HSU	HSU	-	-	-	-	-	-	-
5	5	U	U	-	-	-	-	-	-	-
6	6	HST	HST	-	-	-	-	-	-	-
7	7	T	T	-	-	-	-	-	-	-
8	8	LSW	LSW	-	-	-	-	-	-	-
9	9	LSV	LSV	-	-	-	-	-	-	-
10	10	LSU	LSU	-	-	-	-	-	-	-
11	11	LST	LST	-	-	-	-	-	-	-
12	12	ILS_H	ILS_H	-	-	-	-	-	-	-
13	13	GNDM	GNDM	-	-	-	-	-	-	-
14	14	GNDL	GNDL	-	-	-	-	-	-	-
15	15	LININ	LININ	-	-	-	-	-	-	-
16	-	LINOUT	LINOUT	-	-	-	-	-	-	-
-	16	ILS_L	ILS_L	-	-	-	-	-	-	-
17	17	PTA_7	ADC_SE7	PTA_7	CCTMR1_CH1	MSPWM_CH7	PREDRV_FLT1	UART1_RX	SPI0_SDO	SWD_CLK
18	18	PTA_6	ADC_SE6	PTA_6	CCTMR1_CH0	MSPWM_CH5	PREDRV_FLT0	UART1_TX	SPI0_SCK	SWD_IO
19	19	PTA_5	ADC_SE5	PTA_5	CCTMR0_CH0	MSPWM_CH3	PREDRV_FLT1	UART1_RX	SPI0_SDI	RESET_b
20	20	PTA_4	ADC_SE4	PTA_4	CCTMR0_CH1	MSPWM_CH6	PREDRV_FLT0	UART1_TX	SPI0_SDO	-
21	21	PTA_3	ADC_SE3	PTA_3	CCTMR0_CH1	MSPWM_CH1	PREDRV_FLT1	UART1_RX	SPI0_PCS1	TMU_IN0
22	22	PTA_2	ADC_SE2	PTA_2	CCTMR0_CH0	MSPWM_CH4	PREDRV_FLT0	UART1_TX	SPI0_SDI	TMU_IN1
23	23	PTA_1	ADC_SE1	PTA_1	CCTMR1_CH1	MSPWM_CH2	PREDRV_FLT1	UART1_RX	SPI0_SCK	TMU_OUT
24	24	PTA_0	ADC_SE0	PTA_0	CCTMR1_CH0	MSPWM_CH0	PREDRV_FLT0	UART1_TX	SPI0_PCS0	ZDU_OUT
25	25	VDDA	VDDA	-	-	-	-	-	-	-
26	26	GNDA	GNDA	-	-	-	-	-	-	-
27	27	VDDD	VDDD	-	-	-	-	-	-	-
28	28	VS	VS	-	-	-	-	-	-	-
29	29	CPDRV	CPDRV	-	-	-	-	-	-	-
30	30	VSM	VSM	-	-	-	-	-	-	-
31	31	VBOOST	VBOOST	-	-	-	-	-	-	-
32	32	HSW	HSW	-	-	-	-	-	-	-

7.2 Packages

The packages of YTM32Z1MC0x device are shown as follows:

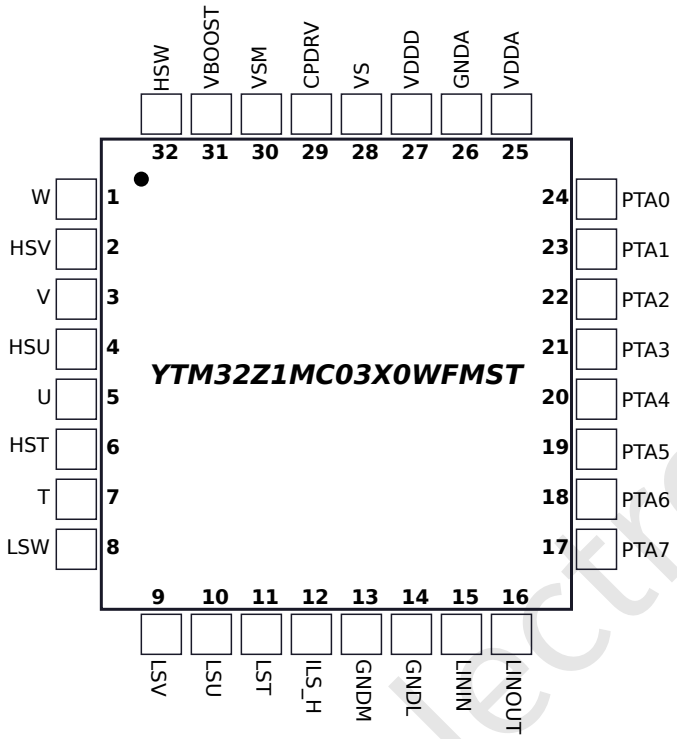


Figure 6: Single End Mode Package

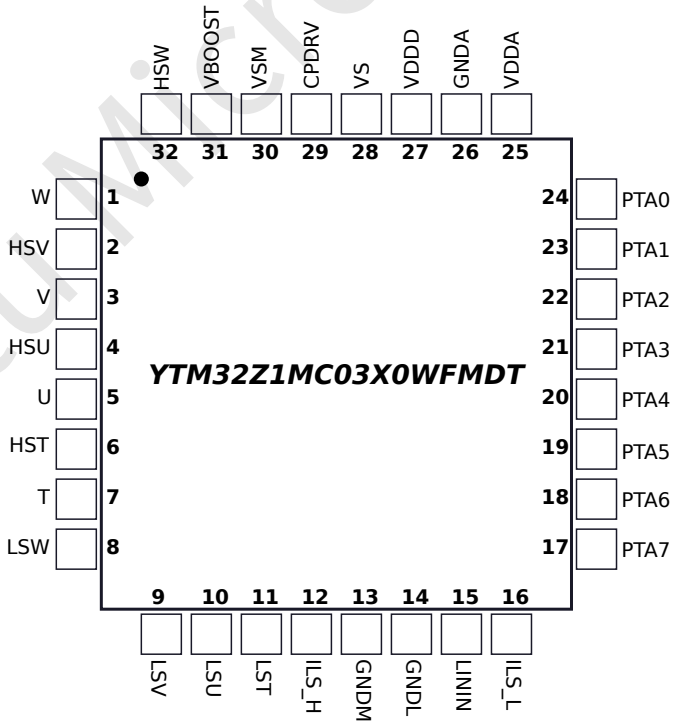
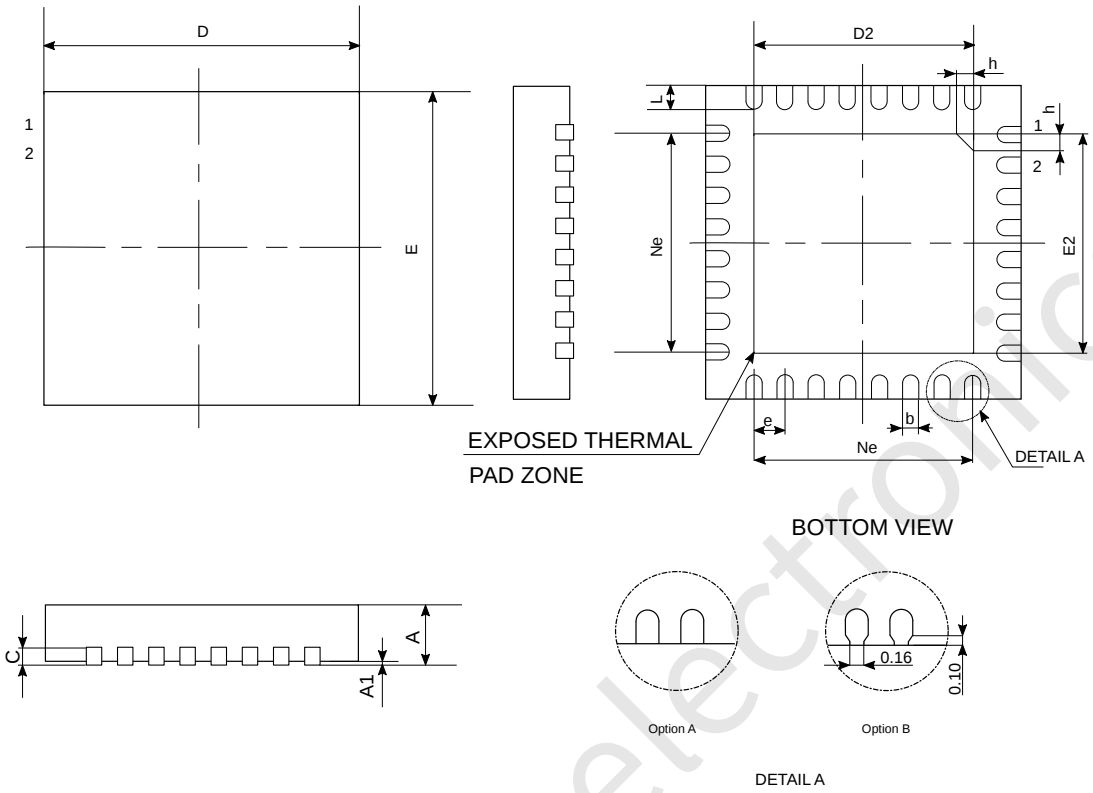


Figure 7: Differential Mode Package

7.3 Dimensions

Package dimensions are as follows:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F	150x150		130x130

Figure 8: 32pin QFN

Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2023/5/17	Initial version

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