YTM32Z1MD0x Data Sheet

Support: YTM32Z1MD04H0MFMDT, YTM32Z1MD04H0MFMT, YTM32Z1MD04H0MFKT

Document Number: YTM32Z1MD0x DS

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1 Features Summary

- AEC-Q100 qualified
- ASIL QM compliant
- RoHS compliant
- ARM Cortex-M0+
  - 32-bit core, running up to 56 MHz
  - Configurable Nested Vectored Interrupt Controller(NVIC)
  - Two-stage pipeline: Reduced number of Cycles Per Instruction(CPI), enabling faster branch instruction and ISR entry, and reducing power consumption
  - Excellent code density in comparison to 8-bit and 16-bit MCUs: Reduced flash size, system cost and power consumption
  - 100 percent compatible with ARM Cortex-M0 and a subset ARM Cortex-M3/M4: Reuse existing compilers and debug tools
  - Simplified architecture: 56 instructions and 17 registers enable easy programming and efficient packaging of 8/16/32-bit data in memory
  - ARM third-party ecosystem support: software and tools to help minimize development time/cost
  - DIVSQRT module with 32-bit integer divide and square root arithmetic operations
- Memory
  - Up to 48KB Program Flash with ECC, supporting Single Error Correction(SEC) and Double Error Detection(DED)
  - Up to 8KB SRAM with ECC, supporting Single Error Correction(SEC) and Double Error Detection(DED)
- Clocks
  - PLL clock, up to 56MHz
  - Slow IRC, up to 2MHz
  - Low power oscillator, run at 10KHz
- Power Management
  - Low power ARM Cortex-M0+ with excellent energy efficiency
  - Support four power modes
    - Active
    - Sleep
    - Deepsleep
    - Deep Powerdown
  - Support clock gating for unused modules, and specific peripherals remain working in Sleep and Deepsleep modes
- Mixed-Signal Analog
  - 5V regulator for >25mA current to supply Hall or Tri-axis position sensor
  - Pre-driver for small NFETs (<50nC@25kHz PWM) to drive BLDC motor
  - On-chip temperature sensor with +/-10°C accuracy
  - Over-current detection, over-voltage and under voltage protection and over temperature protection
  - LIN 2.x/SAE J2602 and ISO17987-4 compliant
  - One 12-bit, up to 1Msps for ILS channel Analog-to-Digital Converter(ADC), which has 32 channels, and 1.5V internal reference
  - One Analog Comparator used for zero-crossing detection in motor driver application
- Communications
  - Up to two Universal Asynchronous Receiver Transmitters(UARTs)
  - One LIN supports LIN 2.x
  - One Serial Port Interface(SPI)
  - Three wakeup sources: LIN, internal wakeup timer and external pin(PTA3)
- Reliability, Safety and Security
  - Internal Watchdog(WDG) with independent clock source
- Timer
  - Capture and Compare Timer(CCTMR): 4 channels
  - Periodic Timer(pTMR)
  - Low Power Timer(lpTMR)
  - Motor Specific Pulse Width Modulation(MSPWM) for a broad range of applications including motor control
- Pre-driver
  - One chargepump for highside gatedrive and one capless ldo for lowside gatedrive
  - Up to three phase pre-driver for small NFETs to drive BLDC motor
  - Over-current detection
  - Over-voltage and under-voltage protection
  - Over-temperature protection
  - Support operational amplifier
  - Zero-cross Detection Unit(ZDU)
- IOs
  - 11 normal IOs for communications, support 5V operation voltage
  - 1 HV IO for wakeup, support 28V voltage input
  - Up to 13 GPIO pins with interrupt functionality
    - 1 GPIO supports high voltage pin (PTA3)
    - 1 GPIO connects to LIN pad
    - 11 normal GPIOs
- HV LDO
  - 1.5V LDO for digital and 5V LDO for analog
- Packages:
  - 32 QFN
  - 24 QFN
- Operating Characteristics
  - Normal operating voltage: 5.5V ~ 28V (operating voltage up to 36V limited to 24h over lifetime)
  - Ambient operation temperature: -40°C ~ 125°C
  - Junction operation temperature: -40°C ~ 150°C

Contents

2 Overview

YTM32Z1MD0x series is an automotive ARM® Cortex®-M0+ MCUs that offers the capability to integrate high voltage analog components. This series integrates high-voltage modules, including the voltage regulator(LDO), Pre-driver and Local Interconnect Network(LIN) physical layer. These features enable a fully integrated single chip solution to drive up to 6 external power MOSFETs for BLDC or PMSM motor drive applications.

3 Block Diagram

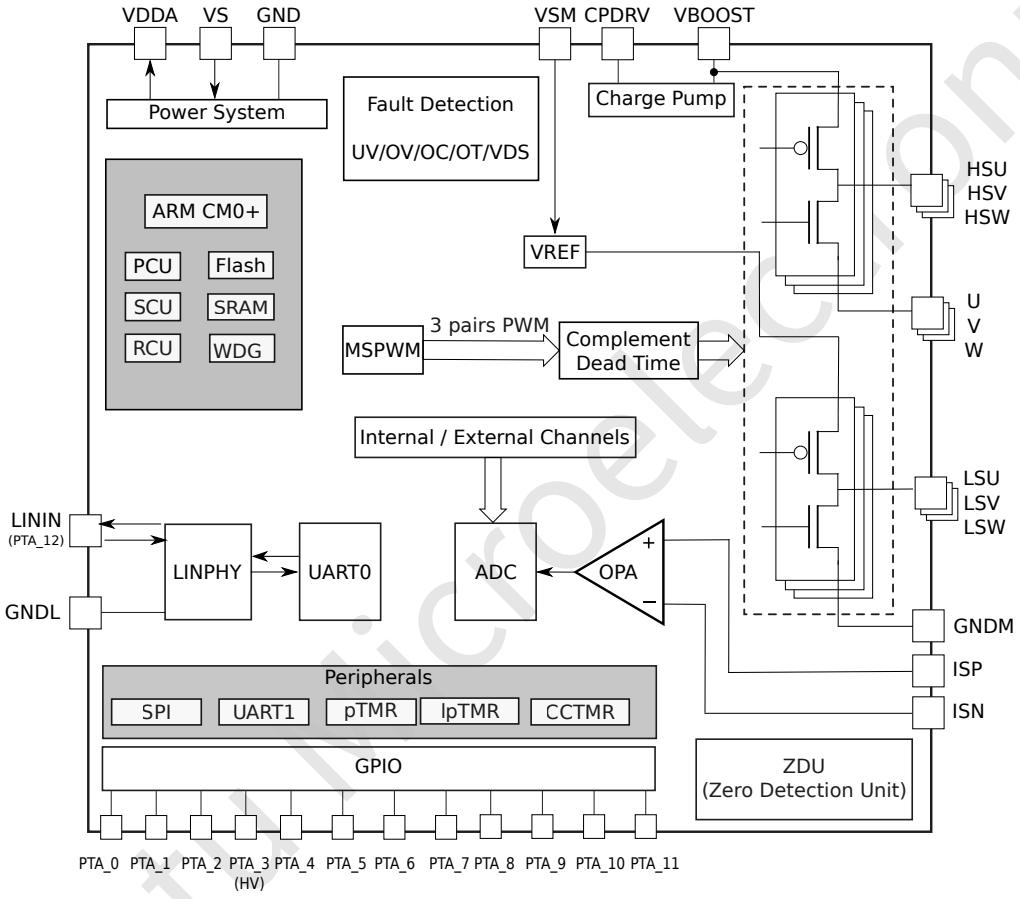


Figure 1: YTM32Z1MD0x Block Diagram

4 Features

The following sections describe the high-level module features for YTM32Z1MD0x device.

4.1 Core Modules

4.1.1 ARM Cortex-M0+

- Up to 56 MHz core frequency
- Supports up to 32 interrupt request sources

- 2 stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the Cortex-M0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Single cycle 32 bits by 32 bits multiplier

4.1.2 Nested Vector Interrupt Controller (NVIC)

- Up to 16 internal interrupt sources and 32 external interrupt sources
- Supports four priority levels for interrupts with two bits in each IPRn registers

4.1.3 Debug Controller

- 2-pin serial wire debug (SWD) provides external debugger interface
- Support JTAG port (IEEE 1149.1 standard)

4.2 System Modules

4.2.1 System Clock Unit (SCU)

- Provide fixed system clock divider to generate bus clock(1/2 frequency of core clock)
- Provide glitch free switcher to select system clock source from OSC and PLL
- Internal RC oscillator(OSC)
  - 2MHz
  - Default system boot clock source
  - PLL reference clock
  - Support working in Deepsleep mode
  - Support trim for temperature and process
- Phase-locked loop(PLL)
  - up to 56MHz
  - Can be selected as system clock source
  - Support working in Deepsleep mode(with OSC working in Deepsleep mode)
  - Contain PLL frequency lock detector, support configurable reset when PLL lock is lost
- Low power oscillator(LPO)
  - 10KHz
  - Can be selected as function clock source
  - Support working in all low power modes including Deep Powerdown mode

4.2.2 Power Control Unit (PCU)

- Combination of internal and external voltage regulator options, offering active and Deep power down mode
- Active POR providing brown-out detect
- Low voltage reset for all system relevant power domains
- VSM under voltage detection with configurable debounce as indication for software
- VSM over voltage monitor with configurable debounce as indication for software
- Over temperature detection with configurable debounce as indication for software
- Over current driving detection with configurable debounce as indication for software
- Wake up source(LIN, PTA3 and LPWDT) in Deep Powerdown mode as indication for software

- Support trim for Iref, bandgap and LDO

4.2.3 Reset Controller Unit (RCU)

- Record the reset sources of most recent resets.
- Configurable filter for reset pin.
- Reset pin filter can work in Active, Sleep, Deepsleep mode.

4.2.4 IP Controller (IPC)

- Peripheral Bus clock enable
- IPC clock source selection from multiple clock sources
- Peripheral software reset

4.2.5 Divide and Square Root (DIVSQRT)

- Lightweight implementation of 32-bit integer divide and square root arithmetic operations.
  - Supports 32/32 signed and unsigned divide (or remainder) calculation
  - Supports 32-bit unsigned square root calculation
- Simple programming model includes registers of input data, result, control, status.
- Programming model interface optimized for activation from inline code or software library call.
  - “Fast Start” configuration minimizes the memory-mapped register write overhead.
  - Supports two methods to determine when the result is valid, including software polling.
  - Configurable divide-by-zero response.
- Pipelined design process 2bits per cycle with early termination exit for minimum execution time.

4.2.6 Trigger Multiplex Unit (TMU)

- Allow software to select the trigger sources for peripherals as trigger sources

4.2.7 Chip Integration Module (CIM)

- System function configuration
- LIN PAD function selection
- CCTMR input capture source selection from ZDU
- Software trigger generate
- Chip and die information

4.3 Memories

4.3.1 Embedded Flash Module (EFM)

- Program Flash (PFlash) support 48KB address space
  - PFlash support ECC 1-bit error correction and 2-bit error detetion (SEC-DED)
- Protection scheme against accidental program or erase operations
- Command protection function for authorization protection
- Optional interruptions on command completion and status update
- Support read buffer to improve AHB read performace

4.3.1.1 Static Random Access Memory (SRAM)

- 8K Bytes SRAM with ECC

4.4 Analog

4.4.1 Analog-to-Digital Converter (ADC)

- Support 12-bit single-ended configurable resolution
- Up to 1Msps for 12-bit resolution conversion performance(for ILS channel only)
- Support up to 30 input channels
  - 13 channels to measure external analog signals from pad
  - 17 channels to measure internal signals
- Support 4 sequences and combination sequences in hardware trigger mode
  - support 4/8/12/16 channels sequence
  - each sequence supports independent trigger source
  - each sequence supports independent sequence mode
- Support two sample time configuration
- Support multiple conversion modes
  - Continuous mode
  - Discontinuous mode
    - Single mode
    - Sequence mode
- Support software/hardware trigger for ADC start conversion
- Support two low power modes
  - Wait mode: prevent ADC overrun when FIFO is full
  - Auto off mode: automatic control ADC power off
- Support watchdog for conversion result monitoring
- Support interrupt generate
  - Sequence trigger miss error event
  - Single trigger miss error event
  - Watchdog event
  - Overrun event
  - End of sequence 3 conversions
  - End of sequence 2 conversions
  - End of sequence 1 conversions
  - End of sequence 0 conversions
  - End of conversion
  - End of sampling
  - ADC ready for conversion

4.4.2 Pre-Driver (PREDRV)

- Drive U/V/W three phases
- Integrate PWM mutex circuit
- Dead time insert
  - Internal pre-driver dead time insert
  - External FET dead time insert
- Fault monitor and safety mechanism
  - Internal fault monitor
    - Under voltage fault

    - Over voltage fault
    - Over current fault
    - Over temperature fault
    - High side and low side VDS fault
  - Customized fault monitor
- Register access protection
- Support operational amplifier
- Interrupt

4.4.3 Zero-cross Detect Unit (ZDU)

- Integrate a comparator internally
- Functional mode
  - Common mode
  - Window mode
- Integrate a virtualize central point internally
- Observation of internal signals by PIN
- Comparator output filter
- Comparator output trigger
- Generate interrupt on rising-edge, falling-edge or both edges of the comparator output

4.5 Timer

4.5.1 Capture Compare Timer(CCTMR)

- Each channel contains a independent 32-bit counter
  - Configurable final counter value
- Support four channel modes
  - Common timer mode
    - Support trigger mode
  - Input capture mode
    - Support common capture mode
    - Support pulse measure mode
    - Support period measure mode
    - Support rising edges, falling edges or dual edges capture
    - Support input filter with a prescaler
  - Output compare mode
    - The output can be configured to set, clear or toggle on match point
  - PWM mode
    - Independent mode for each channel
    - Combination mode to support reloading mechanism
- Support generating triggers
  - Output trigger or window in common timer mode
  - Output capture event in input capture mode
  - Output triggers on match point in ouput compare mode
  - Output pulse with adjustable width in PWM mode
- Support several interrupts
  - Channel function interrupt
  - Counter overflow event interrupt
- Support counter running under debug mode

4.5.2 Motor Specific PWM (MSPWM)

- Contain a 16-bit counter
  - Configurable final counter value
- Support 7-bit clock prescaler
- PWM mode
  - Complementary mode
  - Independent mode
- Support double buffers and registers loading mechanism
- Support double switch logic
- Support generating triggers
  - Output triggers on match point
  - Output window by PWM or related combination logic
- Support several interrupts
  - Channel interrupt
  - Counter overflow interrupt
- Support counter running under debug mode

4.5.3 Periodic Timer (pTMR)

- Timers can generate interrupts, and each channel can generate independent interrupt request
- Four channels of 16-bit timers, each timer has independent timeout periods
- Ability to stop in debug mode
- Support chain mode to connect multiple timer to a longer timer

4.5.4 Low Power Timer (lpTMR)

The features of the lpTMR module include:

- 16-bit time counter or pulse counter with compare
- Optional interrupt can generate asynchronous wakeup from any Low-power mode
- Hardware trigger output
- Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

4.6 Safety

4.6.1 Watchdog (WDG)

- 16-bit countdown timer
- Functional clock can be selected from multiple clock sources
- Support regular or window servicing mode
- Support reset request or interrupt for the first timeout
- Hard and soft configuration lock bits

4.7 Communication Interfaces

4.7.1 Universal Asynchronous Receiver/Transmitter (UART)

- Support LIN break send and detect
- Transmit/Receive buffer
- Baudrate setting
- 1-bit or 2-bit STOP size
- 7-bit, 8-bit, 9-bit or 10-bit frame size
- Transmit/Receive polarity setting
- Receive data match
- Line idle, address match wakeup
- Support transmit/receive line switch
- Support single wire mode

4.7.2 Serial Peripheral Interface (SPI)

- Support clock polarity and phase configuration
- Frame size is 8-bit
- Transmit/Receive 8-bit Buffer.
- Support Standard SPI full-duplex transfer mode and single data line half-duplex transfer mode
- Support Master and Slave mode

4.7.3 Local Interconnect Network Physical Layer (LINPHY)

- Support LIN 2.x standard
- LIN slave controller and transceiver
- Baud rate up to 20Kbps
- Support waking up system by LIN frame
- Support reusing LINPHY pin with CCTMR0, GPIO and UART0

4.8 Human Machine Interface

4.8.1 General Purpose Input/Output (GPIO)

Features of the GPIO module include:

- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- Inversion for data inputs
- Interrupt flag and enable registers for each pin
- Support for edge sensitive (rising, falling, both) or level sensitive (low, high)
- Asynchronous wake-up in low-power modes
- Pin interrupt is functional in all digital pin muxing modes
- Support getting state of the port in all digital pin muxing modes

4.8.2 Port Controller (PCTRL)

The PCTRL module has the following port control features:

- Individual pull control fields with pullup, pulldown, and pull-disable support
- Individual open drain field supporting enable or deisble of the open drain function on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to 14 chip-specific digital functions
- Individual lock function to avoid misoperation

5 Ordering Information

The following chips are available for ordering.

Table 1: Ordering Table

Product	Memory		Package		IO Channel		
Part Number	Flash	SRAM	Pin Count	Package	Normal IO	High Voltage IO	LIN IO
YTM32Z1MD04H0MFMDT	48KB	8KB	32	QFN	7	1	1
YTM32Z1MD04H0MFMT	48KB	8KB	32	QFN	11	1	1
YTM32Z1MD04H0MFKT	48KB	8KB	24	QFN	7	1	1

5.1 Part Number Information

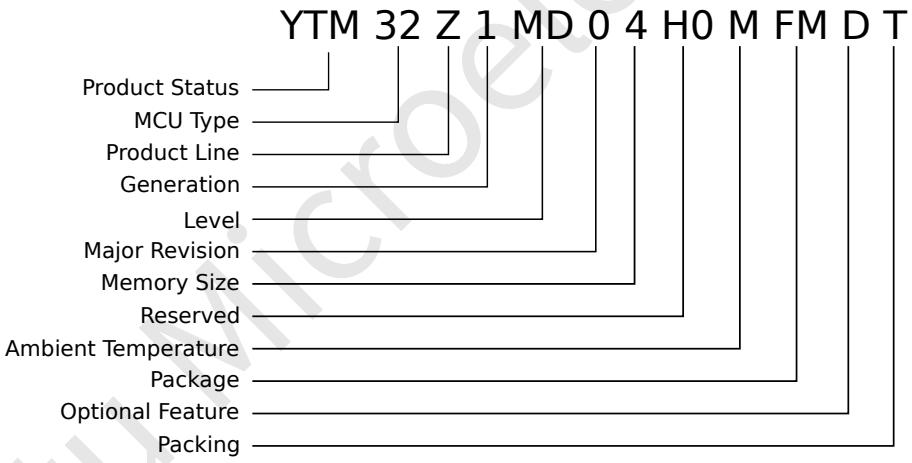


Figure 2: Part Numbers Field

Table 2: Part Number Field Description

Field	Description	Values
YTM	Product Status	YTM: Qualified PTM: Prototype
32	MCU Type	32: 32-bit
B	Product Line	B: General D: Dashboard P: Powertrain V: Vision N: Network Z: High voltage, integrity

Table 2 continued from previous page

Field	Description	Values							
1	Generation	1st generation production							
Hx	Level	Product Line							
		B			Hx: High end Mx: Middle end Lx: Low end				
		Z			Mx: Motor+LIN-PHY Lx: LIN-PHY Cx: CAN-PHY Tx: Touch-sensor Dx: LED Driver				
0	Major Revision	1st revision							
1	Memory Size		0	1	2	3	4	5	6
		Z	-	-	-	32K	48K	64K	128K
		H	1M	2M	4M	6M	8M	12M	16M
		M	-	-	128K	256K	512K	1M	2M
		L	-	-	-	32K	64K	128K	256K
G0	Reserved	Reserved							
M	Ambient Temperature	C: -40°C ~85°C V: -40°C ~105°C M: -40°C ~125°C W: -40°C ~150°C							
LU	Package	Pins			LQFP	QFN	SOP	BGA	
		8			-	-	SB	-	-
		10			-	-	SC	-	-
		12			-	-	SD	-	-
		14			-	-	SE	-	-
		16			-	-	SF	-	-
		20			-	-	SH	-	-
		24			-	FK	-	-	-
		32			LE	FM	-	-	-
		48			LF	FN	-	-	-
		64			LH	FO	-	-	-
		100			LL	-	-	MH	-
		144			LQ	-	-	-	-
		176			LU	-	-	-	-
		208			-	-	-	MK	-
		257			-	-	-	MM	-
		289			-	-	-	MQ	-
		320			-	-	-	MR	-
		373			-	-	-	MS	-
		416			-	-	-	MT	-
		516			-	-	-	MV	-

Table 2 continued from previous page

Field	Description	Values
S	Optional Mode	S: Single end mode D: Differential mode I: ISELED C: Cost Optimization X: ISELED and Cost Optimization
T [1]	Packing	T: Trays/Tubes R: Tape and Reel

1. The chip mark doesn't contain packing information

6 Electrical Characteristics

6.1 Ratings

6.1.1 Thermal Operating Characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ W-Grade\ Part}$	Ambient temperature under bias	-40	–	125	°C
$T_{J\ W-Grade\ Part}$	Junction temperature under bias	-40	–	150	°C

6.1.2 Moisture Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*

6.1.3 ESD Handling Ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model, except LIN pin	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	-500	500	V	
	Corner pins only	-500	500	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C at any pin	-100	100	mA	3
	Latch-up current at ambient temperature of 25 °C at any pin	-200	200	mA	

Table 5 continued from previous page

Symbol	Description	Min.	Max.	Unit	Notes
I_{LAT_DRIVE}	Latch-up current at ambient temperature of 125 °C at drive pin	-250	250	mA	4
	Latch-up current at ambient temperature of 25 °C at drive pin	-250	250	mA	
V_{HBM_LIN}	Electrostatic discharge voltage, human body model, only LIN pin	-6000	6000	V	5

1. Determined according to JEDEC Standard JESD22-A114, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). Equivalent to discharging a 100pF capacitor through a 1.5kΩ resistor.
2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.
3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.
4. @t=10 sec.
5. Determined according to AEC-Q100-002, ESD is applied on LIN pin against shorted GND pins. Equivalent to discharging a 100pF capacitor through a 1.5kΩ resistor.

6.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Limit Min	Max	Unit
Battery supply voltage	V_S		-0.5	28(36V[4])	V
		t < 500 ms	-0.5	45	V
	V_{SM}		V_{DDA}-0.3	28 (36V[4])	V
		t < 500 ms	V_{DDA}-0.3	45	V
	$V_{S.tr1}$	ISO 7637-2 pulse 1[1] V_S=13.5V, T_A=(23 ± 5)°C	-100		V
	$V_{S.tr2}$	ISO 7637-2 pulse 2[1] V_S=13.5V, T_A=(23 ± 5)°C		75	V
	$V_{S.tr3}$	ISO 7637-2 pulse 3A, 3B[1] V_S=13.5V, T_A=(23 ± 5)°C	-150	100	V
Battery supply current	I_{VSM_max}	maximum DC or RMS supply current VSM		125	mA
Output voltage	V_{DDA}		-0.3	5.5	
Output voltage	V_{DDD}		-0.3	1.65	
LIN Bus	V_{LIN}	T < 500ms	-27	45	V
	$V_{BUS.tr1}$	ISO 7637-2 pulse 1[2] V_S=13.5V, T_A=(23 ± 5)°C	-100		V
	$V_{BUS.tr2}$	ISO 7637-2 pulse 2[2] V_S=13.5V, T_A=(23 ± 5)°C		75	V
	$V_{BUS.tr2}$	ISO 7637-2 pulse 3A, 3B[2] V_S=13.5V, T_A=(23 ± 5)°C	-150	100	V
	I_{LIN_max}	Maximum current in LININ	-200	200	mA

Table 6 continued from previous page

Parameter	Symbol	Condition	Limit Min	Max	Unit
Voltage on Analogue HV	V_{ANA_HV}	PTA3 with internal divider T, U, V, W outputs[3]	-0.3	V_S+0.3	V
Voltage on PIN VBOOST	V_{AN_VBOOST}	switching transients at 36V motor drive		45	V
Voltage on Analogue HV	V_{AN_HSx}		-0.3	V_{BOOST}+0.3	V
Voltage on Analogue HV	V_{AN_LSx}		-0.3	V_{REF}+0.3	V
Voltage on pin ILS	V_{ILS_H}, V_{ILS_L}		-0.5	V_{DDA}+0.3	V
Voltage on PTA[7:4] and PTA[2:0]	V_{PTA_LV}		-0.3	V_{DDA}+0.3	V
Voltage on PTA[3]	V_{PTA_HV}		-0.3	V_S+0.3	V
Current on PTA[7:0]	I_{IN_IO}		-10	10	mA

1. ISO 7637 test pulses are applied to V_S via a reverse polarity diode and >22μF/100nF blocking capacitor; ISO 7637 test pulses for 24V car battery needs to be protected by external components.
2. ISO 7637 test pulses are applied to BUS via a coupling capacitance of 1nF; ISO 7637 test pulses for 24V car battery needs to be protected by external components.
3. In case of negative voltages applied on T, U, V, W pins, voltage can go lower than -0.3V.
4. 36V operation is limited to maximum 24 hours over life; 28..36V motor driving may require 100..500 Ohm resistor at VBOOST pin to protect in case of PCB switching transients >45V.

6.3 Peripheral Parameters

6.3.1 Clock Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Frequency of the Internal RC oscillator	F_{rc_osc}	RC oscillator is trimmed	1.98	2	2.02	MHz
Frequency of the PLL	F_{PLL}	RC oscillator is trimmed, and PLL is configured as 40MHz@125°C	35.46	36	36.54	MHz
		RC oscillator is trimmed, and PLL is configured as 56MHz@125°C	55.16	56	56.84	MHz
Settling time of the PLL	T_{setPLL}	RC oscillator is trimmed, and PLL is switched on		2		ms
Frequency of the low power oscillator	F_{lpo_clk}		7.8	10	14	KHz
Startup time of the system after power on	T_{por}	C_{VDDA}=C_{VDDD}=100nF; time until the first Flash instruction can be executed.			TBD	ms

Table 7 continued from previous page

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Startup time of the Charge pump	T_{pump}	Time from Charge pump start till V_{BOOST}=V_S+6V for V_S>12V; motor not running during startup, C_{fly}=100nF, C_{BOOST}=1μF			5	ms

6.3.2 Regulator Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Voltage supply	Vs		6	14	28	V
5V regulator	V_{DDA}	After trimmed	4.85	5	5.15	V
Output current capability	I_{DDout_vdda}				55	mA
1.5V regulator	V_{DDD}	After trimmed	1.44	1.5	1.56	V
Output current capability	I_{DDout_vddd}				27	mA

6.3.3 Power Mode Transition Operating Behaviors

Description	System clock	Frequency	Min.	Typ.	Max.
SLEEP -> ACTIVE	PLL	56MHz	–	90ns	–
DEEPSLEEP -> ACTIVE	PLL	56MHz	–	2.057ms	–
DEEPPOWERDOWN -> ACTIVE	OSC	2MHz	–	283μs	–
T_{POR}	OSC	2MHz	–	68.96μs	–

6.3.4 Power Consumption

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max	Unit
ACTIVE	I_{DD_ACTIVE}	PLL	Running coremark in flash, all peripheral clock enabled. core @56MHz, bus @28MHz V_S=12V	25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA
			Running coremark in flash, all peripheral clock disabled. core @56MHz, bus @28MHz V_S=12V	25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @56MHz, bus @28MHz V_S=12V	25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA

Table 10 continued from previous page

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max	Unit
			Running while(1) loop in flash, all peripheral clock disabled. core @56MHz, bus @28MHz V_S=12V	25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA
		OSC	Running coremark in flash, all peripheral clock enabled. core @2MHz, bus @1MHz V_S=12V	25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA
			Running coremark in flash, all peripheral clock disabled. core @2MHz, bus @1MHz V_S=12V	25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA
			Running while(1) loop in flash, all peripheral clock enabled. core @2MHz, bus @1MHz V_S=12V	25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA
			Running while(1) loop in flash, all peripheral clock disabled. core @2MHz, bus @1MHz V_S=12V	25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA
SLEEP	I_{DD_SLEEP}	PLL	Sleep mode current, core @2MHz, bus @1MHz V_S=12V	≤ 25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA
DEEPSLEEP	$I_{DD\_DEEPSLEEP}$	PLL	Deepsleep mode current, V_S=12V OSC, PLL enable	≤ 25 °C	–	TBD	–	mA
				150 °C	–	TBD	–	mA
			Deepsleep mode current, V_S=12V OSC enable, PLL disable	≤ 25 °C	–	TBD	–	μA
				150 °C	–	TBD	–	μA
			Deepsleep mode current, V_S=12V OSC, PLL disable	≤ 25 °C	–	TBD	–	μA
				150 °C	–	TBD	–	μA
DEEP POWERDOWN	$I_{DD\_DEEPPOWERDOWN}$	PLL	Deep Powerdown mode current, V_S=12V	≤ 25 °C	–	TBD	–	μA
				150 °C	–	TBD	–	μA

6.3.5 IO Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Leakage current in PTA[11:0]	I_{leakio}	1/16 divider on PTA3 disabled	-5		5	μA
Digital high input threshold level	V_{ih}		0.7*VDDA			V
Digital low input threshold level	V_{il}				0.3*VDDA	V
Digital input hysteresis	$V_{inhystio}$		0.1*VDDA			V
PTA3 wakeup threshold level	V_{wu_lh}	Active in Deep Powerdown mode	0.7*VDDA			V
PTA3 wakeup threshold level	V_{wu_hl}	Active in Deep Powerdown mode			0.3*VDDA	V
PTA3 wakeup hysteresis	V_{hystio_wu}	Active in Deep Powerdown mode	0.1*VDDA			V
Output voltage low	V_{outl_pta}	PTA[11:4,2:0], I_{load}=3mA			0.4	V
Output voltage high	V_{outh_pta}	PTA[11:4,2:0], I_{load}=-3mA	VDDA - 0.4			V
Output voltage low	V_{outl_pta3}	PTA3, I_{load}=10mA			0.4	V
Input voltage range for ADC	$V_{in\_adc\_pta[11:4,2:0]}$	For information only	0		4	V
Input voltage range for ADC	$V_{in\_adc\_pta3}$	For information only	0		36	V

6.3.6 ADC Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
ADC VREF	–	–		1.5		V
ADC full scale range	–	–	0		4	V
Differential nonlinearity	DNL	Only characterized; no production tset	-1		1	LSB
Integral nonlinearity	INL	Only characterized; no production tset	-3		3	LSB
Minimum conversion time	T_{conv}	function clock=30MHz	0.625			μs
Minimum sampling time	T_{samp}	Time between channel select and start of conversion	0.375			μs
Channel set up time	T_{setup}	With channel change	3			μs
Minimum time between 2 ADC conversions	T_{cycl}	function clock=30MHz; without channel change	1			μs
		with channel change	4			μs
ADC error(excluding ADC reference and INL)	Err_{ADC}	LV channels	-1		1	%
		HV channels(with predivider)	-3		3	%
Temperature sensor accuracy	ACC_{tempS}		10		-10	°C

Table 12 continued from previous page

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Slope of temperature and voltage curve	K[1]	ADC sampling frequncy @ 500kHz		267		

1. T = C - K*V, see Reference Manual for details.

Table 13: Current Sense Amplifier

Parameter	Conditions	Value			Unit
		Min.	Typ.	Max.	
Current sense amplifier gain	bit = 00		4		
	bit = 01		8		
	bit = 10 (default)		16		
	bit = 11		32		
Current sense amplifier input range	bit = 00	-300		300	mV
	bit = 01	-150		150	mV
	bit = 10	-75		75	mV
	bit = 11	-37.5		37.5	mV
Current sense amplifier gain error		-5%		+5%	
Current sense amplifier series resistor	On-die resistor for external channels		10k		
Current sense amplifier external cap	External filter cap for external channels		100n		

6.3.7 Voltage Detect Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
POR off	V_{por_lh}	Only for information	1.74	2	2.23	V
POR on	V_{por_hl}	Only for information	1.52	1.83	2.11	V
Hysteresis for POR	V_{hyst_por}	Only for information		170		mV
VSM Programmable range for undervoltage level	V_{uv_range}	LVDT_VSM_CFG[2:0]=000	3.5	4	4.5	V
		LVDT_VSM_CFG[2:0]=001	4.5	5	5.5	V
		LVDT_VSM_CFG[2:0]=010	5.5	6	6.5	V
		LVDT_VSM_CFG[2:0]=011	6.5	7	7.5	V
		LVDT_VSM_CFG[2:0]=100	7.5	8	8.5	V
		LVDT_VSM_CFG[2:0]=101	8.5	9	9.5	V
Hysteresis for VSM undervoltage detect	V_{hyst_uv}			0.5		V

Table 14 continued from previous page

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Debouncing for VSM undervoltage detect	T_{uv}	Only for information		5		μs
VDDA undervoltage reset on	$V_{uvr\_hl\_VDDA}$			2.7		V
VDDA undervoltage reset off	$V_{uvr\_lh\_VDDA}$			2.88		V
Hysteresis for undervoltage reset	$V_{hyst\_uvr\_VDDA}$	Guaranteed by design	0.18			V
Debouncing for VDDA undervoltage reset	T_{uvr_VDDA}			2.7		μs
VDDD undervoltage reset on	$V_{uvr\_hl\_VDDD}$			1.275		V
VDDD undervoltage reset off	$V_{uvr\_lh\_VDDD}$			1.325		V
Hysteresis for undervoltage reset	$V_{hyst\_uvr\_VDDD}$	Guaranteed by design		0.05		V
Debouncing for VDDD undervoltage reset	T_{uvr_VDDD}			2.7		μs

6.3.8 Tempsensor Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Over temperature shutdown interrupt	T_{ot_on}	Tested by special test mode	155	160	165	°C
	T_{ot_off}		130	135	140	°C
	T_{ot_hyst}	Guaranteed by design	25			°C
Temperature range	T_{range}	Sensor measures IC junction temperature	-40		180	°C
Temperature measurement gain	T_{temp_gain}			0.26		°C/LSB
Accuracy	T_{acc}	Guaranteed by design, after calibration	-10		10	°C

6.3.9 VSM Sensor Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input range	VSM_max				36	V
Output capability	$T_{settling\_ADC}$	Time to charge the ADC sampling capability, only information, no production test		2.5		μs
Low-pass filter cut-off frequency	F_{vsm_filter}	-3dB cutoff frequency, only information	1.9		3.6	kHz
VSM sensor filter offset	$V_{adc\_vsm\_offset}$	Referred to input voltage of VSM	-400		400	mV

6.3.10 PREDRV Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Low side FET gatedrive voltage	V_{REF_LS}	$V_{SM} \geq 7V$	7	9	10	V
		$5V<V_{SM}<7V$	V_{SM}-1			V
Low side Ron charge	R_{LS_HIGH}	$V_S=V_{SM}=8\sim36V$, test at 13V in production	4	6	12	Ω
Low side Ron discharge	R_{LS_LOW}	$V_S=V_{SM}=8\sim36V$, test at 13V in production	1	2	8	Ω
High side Ron charge	R_{HS_HIGH}	$V_S=V_{SM}=8\sim36V$, test at 13V in production	4	6	12	Ω
High side Ron discharge	R_{HS_LOW}	$V_S=V_{SM}=8\sim36V$, test at 13V in production	1	2	8	Ω
Chargepump output voltage	V_{BOOST}	$V_{SM} \geq 10V$	V_{SM}+7.5	V_{SM}+8.8	V_{SM}+10	V
		$8V \leq V_{SM}<10V$	V_{SM}+5.5		V_{SM}+9.5	V
		$5.5V<V_{SM}<8V$	V_{SM}+3.5		V_{SM}+8	V
CPDRV output resistance	R_{CPDRV_HIGH}	I_{load}=2mA, test at 13V in production	15	40	120	Ω
	R_{CPDRV_LOW}	I_{load}=2mA, test at 13V in production	10	26	60	Ω
	F_{CP_FREQ}		45	60	75	kHz
Dead time	T_{DEAD}	Programmable with 8 bits.	0	1.0	5.3	μs
Predrv current sensor input range	V_{CURR_IR}	Allowed input range of shunt voltage, for information only	-300		300	mV
Current sensor gain	A_{cs}		4	16	32	
Current sensor reference	V_{cs0}	V_{ILS}=0(the value of common-mode voltage)		1.5		V
Current sensor calibration error	V_{cs_err}	Measured at the output of the current sensor	TBD		TBD	mV
Current sensor low	T_{cs_filter}	Guaranteed by design	0.25	0.5	1	μs
Overcurrent detection	V_{oc}		10	300	400	mV
VDS over-voltage level	VTH_OV_VDS_0	VDSMON_VTH_SEL = 00	0.3	0.5	0.7	V
	VTH_OV_VDS_1	VDSMON_VTH_SEL = 01	0.8	1.0	1.2	V
	VTH_OV_VDS_2	VDSMON_VTH_SEL = 10	1.3	1.5	1.7	V
	VTH_OV_VDS_3	VDSMON_VTH_SEL = 11	1.8	2.0	2.2	V
VDS over-voltage hysteresis level	VHYS_VDS		0.04		0.22	V
Filter Time	T_{vds}	Time from FET on till V_{ds} monitoring start. Programmable with 8 bits.	0	1.6	5.3	μs

Table 17 continued from previous page

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input common voltage of zero-detect comparator	V_{cm_zdc}		-0.1		1.5	V
Delay of zero-detect comparator	T_{zdc_dly}				1.5	μs

6.3.11 LIN Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Short circuit bus current	I_{BUS_LIM}	V_{BUS}=V_{BAT}=18V, driver on	40		200	mA
Pull up resistance bus, normal and standby mode	R_{SLAVE}		20		60	kΩ
Pull up current, sleep mode	$I_{LIN\_PU\_SLEEP}$	V_{BUS}=0V, V_{BAT}=12V, sleep mode	-100			μA
Input leakage at the receiver incl.PU	$I_{BUS\_PAS\_dom}$	V_{BUS}=0V, V_{BAT}=12V	-1			mA
		V_{BUS}=0V, $V_{BAT=24V}$	-2			mA
Bus reverse current, recessive	$I_{BUS\_PAS\_rec}$	Driver off, 8V<V_{BAT} $\leq$ 27V			20	μA
		27V< V_{BAT}<36V			50	μA
Bus reverse current, loss of battery	$I_{BUS\_NO\_BAT}$	V_S=0V, 0V<V_{BUS}<18V		1	23	μA
		18V< V_{BUS}<36V			100	μA
Bus current during loss of ground	$I_{BUS\_NO\_GND}$	V_S=V_{GND}=12V, V_{BUS}=0V $\sim$ 18V	-1		1	mA
		V_S=V_{GND}=24V, V_{BUS}=0V $\sim$ 36V	-2		2	mA
Transmitter dominant voltage	V_{olbus}	Network load=500Ω, TxD=0	0		0.2	VS
Transmitter recessive voltage	V_{ohbus}	TxD open	0.8		1	VS
BUS input capacitance	C_{BUS}	Only information		25	35	pF
Receiver dominant voltage	V_{BUSdom}				0.4	VS
Receiver recessive voltage	V_{BUSrec}		0.6			VS
Centre point of receiver threshold	V_{BUS_CNT}	V_{BUS_CNT}=(V_{BUSdom}+V_{BUSrec})/2	0.475	0.5	0.525	VS
Receiver hysteresis	V_{BUS_hys}	V_{BUS_hys}=V_{BUSres}-V_{BUSdom}	0.15		0.175	VS
Propagation delay receiver[125]	T_{rx_pdf}	$C_{RxD=25pF}$ Falling edge			6	us
Propagation delay receiver[125]	T_{rx_pdr}	$C_{RxD=25pF}$ Rising edge			6	us

Table 18 continued from previous page

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Propagation delay receiver symmetry[5]	T_{rx_sym}	T_{rx_pdf} - T_{rx_pdr}	-2		2	us
Receiver debounce time[6]	T_{rec_deb}	LIN rising and falling edge	0.5		4	us
LIN duty cycle 1[2][3]	D1	20kbps operation, normal mode	0.396			
LIN duty cycle 2[2][3]	D2	20kbps operation, normal mode			0.581	
LIN duty cycle 3[2][3]	D3	10.4kbps operation, low speed mode	0.417			
LIN duty cycle 4[2][3]	D4	10.4kbps operation, low speed mode			0.59	
$T_{rec(max)}$ - $T_{dom(min)}$ [4]	Δt3	10.4kbps operation, low speed mode			15.9	μs
$T_{rec(min)}$ - $T_{dom(max)}$ [4]	Δt4	10.4kbps operation, low speed mode			17.28	μs

1. This parameter is tested by applying a square wave signal to the LIN. The access to internal signals RxD, TxD will be performed by test mode. The minimum slew rete for the LIN rising and falling edge is 50V/μs.
2. See Figure3:LIN timing diagram
3. Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal termination disabled
4. In accordance to SAE J2602
5. Parameter in relation to internal signal TxD
6. Internal value to suppress spikes; only proved during characterization:not measured in production

As shown in figure, both worst case duty cycles can be calculated as follows:

$$D_{wc1} = t_{BUS\_Rec(min)}/2 * t_{Bit}$$
$$D_{wc2} = t_{BUS\_Rec(max)}/2 * t_{Bit}$$

Thresholds for duty cycle calculation in accordance to LIN2.x:

Baud rate	20kBaud	10.4kBaud
t_{Bit}	50μs	96μs
D_{wc1}	D1	D3
D_{wc2}	D2	D4
$TH_{REC(MAX)}$	0.774 V_{S_TX}	0.778 V_{S_TX}
$TH_{DOM(MAX)}$	0.581 V_{S_TX}	0.616 V_{S_TX}
$TH_{REC(MIN)}$	0.422 V_{S_TX}	0.389 V_{S_TX}
$TH_{DOM(MIN)}$	0.284 V_{S_TX}	0.251 V_{S_TX}

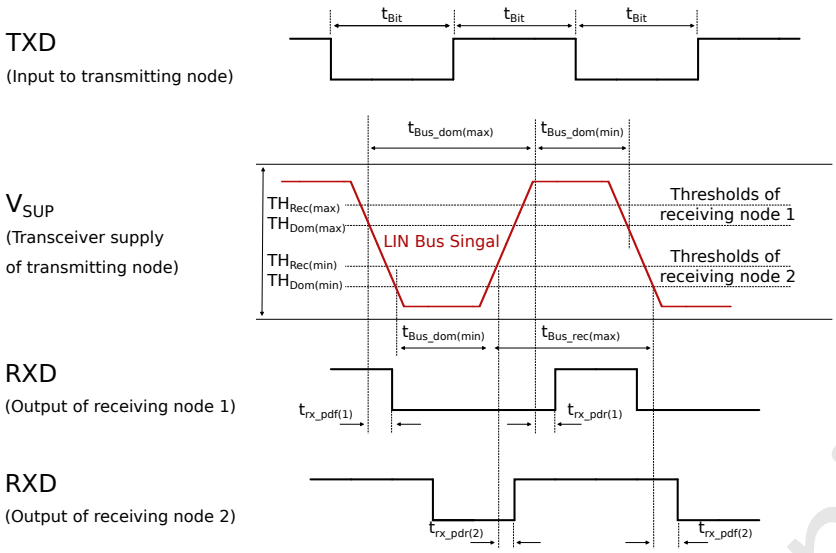


Figure 3: LIN Timing Diagram

6.3.12 NVM Flash Parameters

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Write time for 64-bit data	T_{write}		74.7	83.7	88.1	us
Sector erase time	T_{erase_sec}		4.67	5.17	5.66	ms
Block erase time	T_{erase_blk}		20.67	30.66	40.66	ms
Read access time	T_{acc}	Tj=-40°C ~ 125°C		40		ns
Read temperature	T_{read_fls}		-40		125	°C
Program and erase temperature	T_{pg_fls}		-40		125	°C
Cycling endurance	$T_{nvmcycp}$	Tj@125°C	20000			cycle
Data retention	T_{nvmret}	Tj@25°C	100			years
		Tj@85°C	25			years
		Tj@125°C	10			years

6.3.13 Debug Module Electrical

6.3.13.1 SWD Electrical Specifications

Table 21: SWD Full Voltage Range Electricals

Symbol	Description	Min.	Typ.	Max.	Unit
T1	SWD_CLK frequency	–	–	20	MHz
T2	SWD_CLK cycle period	50	–	–	ns
T3	SWD_CLK pulse width	20	–	–	ns

Table 21 continued from previous page

Symbol	Description	Min.	Typ.	Max.	Unit
T4	SWD_CLK rise and fall time	–	–	3	ns
T5	SWD_CLK input data setup time to SWD_CLK rise edge	8	–	–	ns
T6	SWD_CLK input data hold time after SWD_CLK rise edge	1.5	–	–	ns
T7	SWD_CLK high to SWD_DIO output data valid	–	–	35	ns
T8	SWD_CLK high to SWD_DIO output data Hi-Z	5	–	–	ns

6.3.13.2 SWD Input Clock Timing

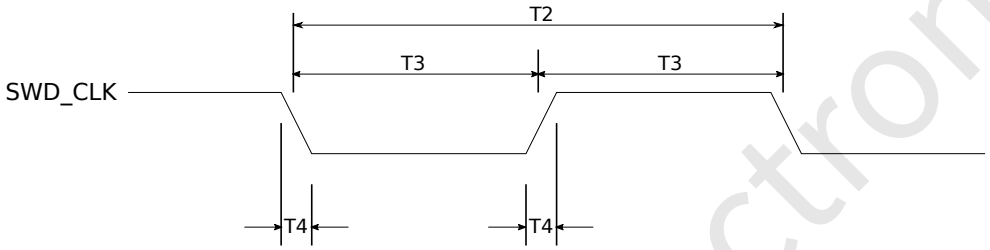


Figure 4: SWD Clock Timing

6.3.13.3 SWD Output Data Timing

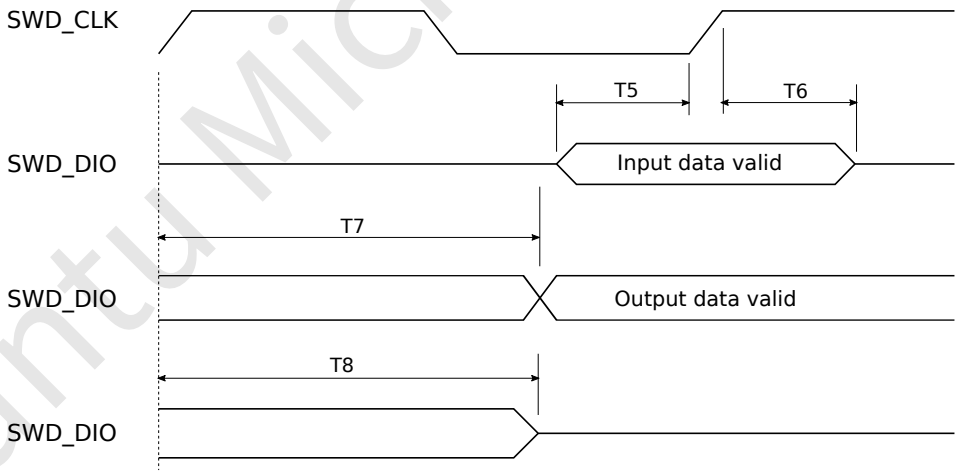


Figure 5: SWD Data Timing

6.4 Thermal Attributes

Table 22: Thermal Characteristics

Package Family	Package Type	Thermal Resistance JA (°C/W)
QFN	QFN32L	41
	QFN24L	52

7 Pinouts

7.1 IO Signal Description

The pinouts signal description is as follows:

Table 23: Pinmux Table

32QFN (#1)	32QFN (#2)	24QFN	NAME	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15
32	1	1	HSW	HSW	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
1	2	2	W	W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
2	3	3	HSV	HSV	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
3	4	4	V	V	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
4	5	5	HSU	HSU	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5	6	6	U	U	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
6	-	-	NC	NC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
7	-	-	NC	NC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
8	7	7	LSW	LSW	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
9	8	8	LSV	LSV	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
10	9	9	LSU	LSU	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
11	-	-	NC	NC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
12	10	10	ISP	ISP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	11	11	ISN	ISN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
13	12	12	GNDM	GNDM	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
14	-	-	GNDL	GNDL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	13	13	LININ	LININ	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
16	-	-	ISN	ISN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	14	-	NC	NC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	15	-	PTA_9	ADC_SE9	PTA_9	CCTMR0_CH2	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS1	-	lpTMR_ALT1	PREDRV_FLT1	-	-	TMU_OUT2	-
-	-	-	VPP	VPP	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	16	-	PTA_8	ADC_SE8	PTA_8	CCTMR0_CH3	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS1	-	lpTMR_ALT1	PREDRV_FLT0	-	-	TMU_OUT3	-
17	17	14	PTA_7	ADC_SE7	PTA_7	CCTMR0_CH3	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS0	-	lpTMR_ALT1	PREDRV_FLT1	MSPWM_CH0	MSPWM_CH5	TMU_OUT0	SWD_CLK
18	18	15	PTA_6	ADC_SE6	PTA_6	CCTMR0_CH2	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS0	-	lpTMR_ALT1	PREDRV_FLT0	MSPWM_CH2	MSPWM_CH1	TMU_OUT1	SWD_IO
19	19	16	PTA_5	ADC_SE5_SB	PTA_5	CCTMR0_CH1	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS0	-	lpTMR_ALT1	PREDRV_FLT1	MSPWM_CH4	MSPWM_CH3	MCU_CLKOUT	MCU_Reset_b
20	20	17	PTA_4	ADC_SE4_FB_UVW_TEST	PTA_4	CCTMR0_CH0	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS0	-	lpTMR_ALT1	PREDRV_FLT0	-	-	TMU_OUT2	MCU_CLKOUT
21	21	18	PTA_3	ADC_SE3	PTA_3	CCTMR0_CH0	-	-	-	-	-	-	-	lpTMR_ALT1	PREDRV_FLT1	-	-	TMU_IN0	-
22	22	-	PTA_2	ADC_SE2_VN_TEST	PTA_2	CCTMR0_CH1	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS0	-	lpTMR_ALT1	PREDRV_FLT0	MSPWM_CH1	MSPWM_CH4	TMU_IN0	-
23	23	-	PTA_1	ADC_SE1	PTA_1	CCTMR0_CH2	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS0	-	lpTMR_ALT1	PREDRV_FLT1	MSPWM_CH3	MSPWM_CH0	TMU_IN1	-
24	24	-	PTA_0	ADC_SE0	PTA_0	CCTMR0_CH3	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS1	-	lpTMR_ALT1	PREDRV_FLT0	MSPWM_CH5	MSPWM_CH2	TMU_IN1	-
-	25	-	PTA_11	ADC_SE11	PTA_11	CCTMR0_CH0	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS1	-	lpTMR_ALT1	PREDRV_FLT1	-	-	TMU_OUT0	-
-	26	-	PTA_10	ADC_SE10	PTA_10	CCTMR0_CH1	UART1_RX	UART1_TX	SPI0_SDO	SPI0_SCK	SPI0_SDI	SPI0_PCS1	-	lpTMR_ALT1	PREDRV_FLT0	-	-	TMU_OUT1	-
-	-	-	VDDD	VDDD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	VDDIO5	VDDIO5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
25	27	19	VDD5	VDD5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	GNDD	GNDD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	GNDA	GNDA	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
26	28	20	GND	GND	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
27	-	-	VDDD	VDDD	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
28	29	21	VS	VS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
29	30	22	CPDRV	CPDRV	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
30	31	23	VSM	VSM	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
31	32	24	VBOOST	VBOOST	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

7.2 Packages

The information of package pinouts is as follows:

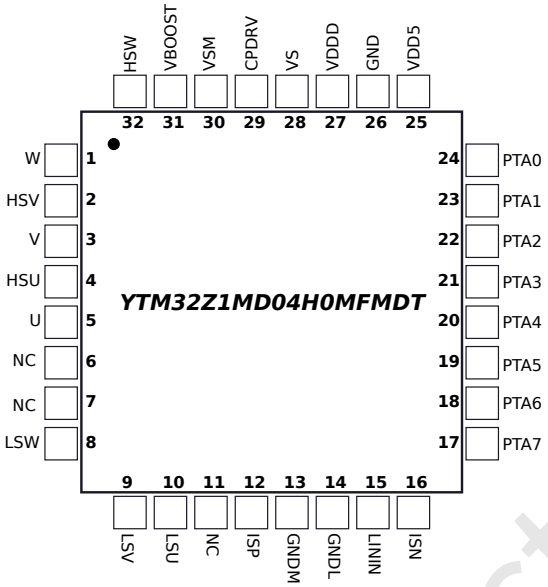


Figure 6: 32QFN(1) Package

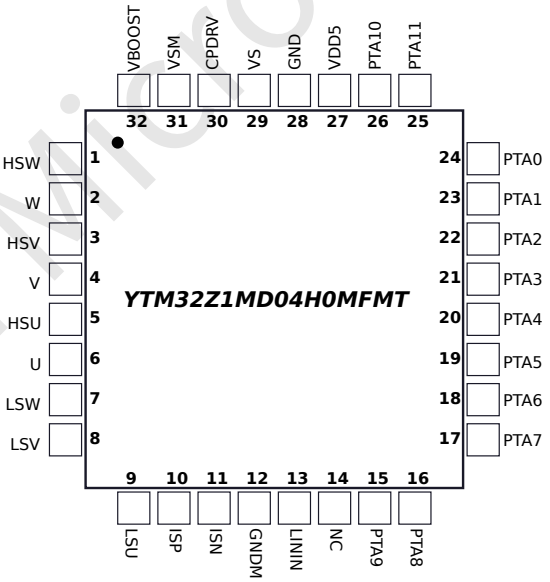


Figure 7: 32QFN(2) Package

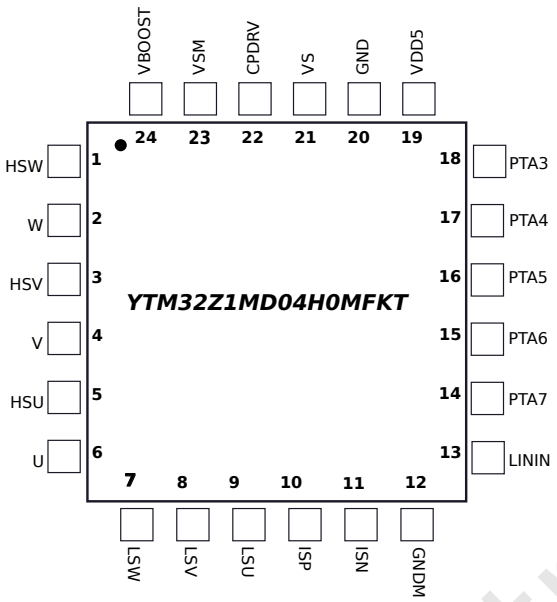
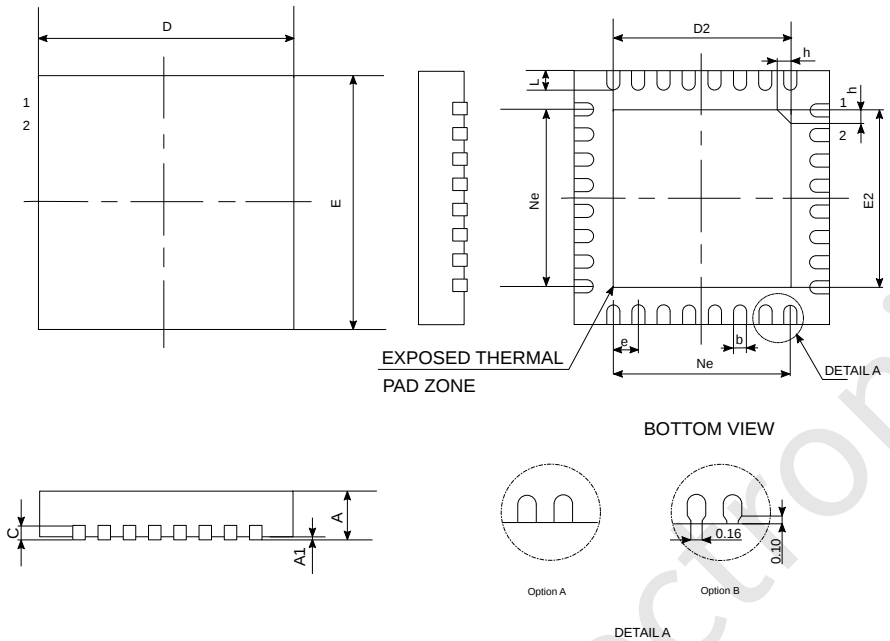


Figure 8: 24QFN Package

Note: The chip mark will not contain packing information(T/R)

7.3 Dimensions

Package dimensions are as follows:



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F	150x150		130x130

Figure 9: 32pin QFN

Revision History

The following table provides a revision history for this document.

Rev.No.	Date	Substantive Change(s)
1.0	2024/2/2	Initial version

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